ADM-PB125
User Manual

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1 Introduction

The ADM-PB125 is a high-performance reconfigurable computing card featuring the latest AMD Adaptive Compute Acceleration Platform (ACAP) platform known as Versal. The PCIe form factor is ideal for Data Center applications and general evaluation and deployment of this architecture. The card features three QSFP-DD interfaces, four banks of 8GB LPDDR4-SDRAM, front panel Ethernet, 1PPS input, 10MHz input, trigger I/O, RJ45 ToD/1PPS, PMOD, and USB.

Figure 1 : ADM-PB125 Fully Assembled

1.1 Order Code

See the datasheet on web page https://www.alpha-data.com/product/adm-PB125/ for complete ordering options.

1.2 Key Features

Key Features

- PCIe Gen4 x16, dual Gen5x8 capable
- 2-slot active or passive heat sink
- 1-slot build available upon request
- 3/4 length, full profile, x16 edge PCIe form factor
- Supports Versal XCVP2502-2MSE and XCVP2502-3HSE in the VSVB3340 package
- 3x QSFP-DD interfaces at front panel
  - 2x QSFP-DD cages connected to GTM capable of 56g PAM4 on each of the 16 channels.
  - 1x QSFP-DD cage connected to GTY capable of 28g NRZ on each of the 8 channels.
- Industry standard low speed I/O at the front panel
  - SMA for 1PPS input
  - SMA for 10MHz input
  - SMA with Trig input/output
  - RJ45 with 2x bidirectional RS485 interfaces for ToD and 1PPS
- Versatile MIO interface support:
  - GEM0 Ethernet access through RJ45 at front panel
  - uSD
  - Dual QSPI
  - ULPI USB PHY accessible at rear USBA receptacle
  - 2x UART accessible through micro-USB at PCIe front panel and rear
- Four separate banks of 8GB LPDDR4 SDRAM at 3933 MT/s
- Front panel and rear edge JTAG access via micro-USB ports
- ACAP configurable over JTAG and SPI configuration flash
- Voltage, current, and temperature monitoring
- Digilent PMOD 3.3V, 12-pin interface accessible to PL
- 6 user LEDs

2 Board Information

2.1 Physical Specifications

The ADM-PB125 complies with PCI Express CEM revision 5.0.

Description	Measure
PCB Dy	111.15 mm
PCB Dx	254 mm
Total Dz	19.9 mm

Table 1 : Mechanical Dimensions (PCB only)

Description	Measure
Total Dy	126.3 mm
Total Dx	267.5 mm
Total Dz	41.9 mm
Total weight	TBD grams
Weight of PCIe handle	30 grams

Table 2 : Mechanical Dimensions (Fully Assembled)

The total weight does not include the PCIe Handle, which is optional, and shipped uninstalled.

2.2 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

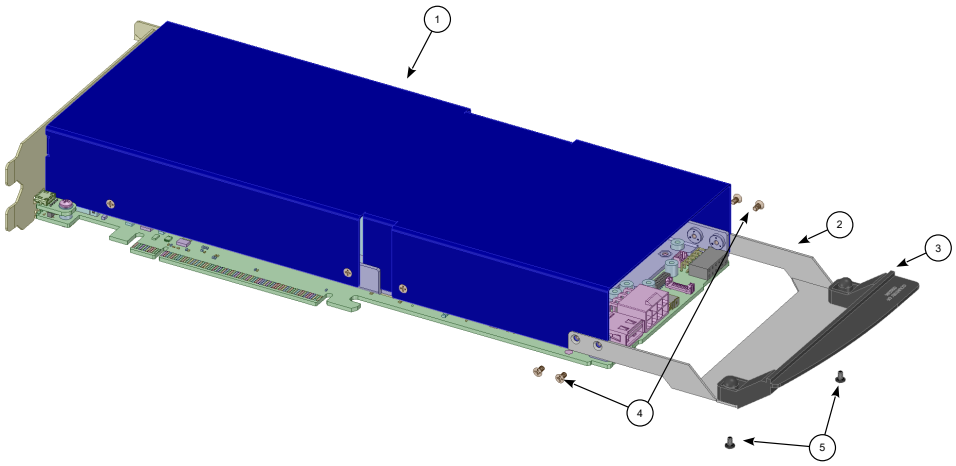
2.3 PCIe Handle Installation

The ADM-PB125 ships fully assembled. There is a PCIe-compliant handle shipped in a separate bag within the product package. This handle assembly includes a plastic handle and a metal bracket. The bracket simulates the full-length PCIe card length and lines up with common server retention clips. The plastic handle can be removed and only the metal bracket used if it fits better in the host system. Use all retention options available to secure this add-in card.

The drawing below details the installation of the rear handle bracket.

ITEM	PART NO	DESCRIPTION	QTY	MANUFACTURER/DISTRIBUTOR
1	ADM-PB125	ADM-PB125 (AD01533), PCIE, ASSEMBLY	1	ALPHA DATA
2	AD01398-1_SP05-3	HANDLE SUPPORT BRACKET (GOMPF P/N 3200-2954LC ECO 02)	1	GOMPF
3	91060000AFG	PCIE HANDLE	1	GOMPF
4	92010A001	SCREW, M2 X 4MM, FLAT HEAD, STAINLESS STEEL	4	MCMASTER-CARR / GENERIC
5	6089-3512	SCREW, SELF-THREADING, PAN HEAD, STAINLESS STEEL	2	GOMPF

REV	ZONE	DESCRIPTION	DATE	DWN BY
1	ALL	INITIAL RELEASE	07-JUL-2025	J. WOOD



NOTES
1. USE LOCTITE 222 ON ALL SCREWS
2. TORQUE ALL SCREWS TO 0.23N-M [2IN-LBS].
3. SUGGESTED ASSEMBLY ORDER FOLLOWS ITEM NUMBER IN ASCENDING ORDER.
4. START ALL SCREW SETS LOOSELY BEFORE TIGHTENING GROUP.

Alpha Data Parallel Systems Ltd
Title: ADM-PB125 Support Bracket Assembly
Size: A2 | Document No: AD01533-1_FA03-1 | Rev: 1

Figure 2 : ADM-PB125 PCIe Handle Installation

2.4 Chassis Requirements

2.4.1 PCI Express

The ADM-PB125 is capable of PCIe Gen 1/2/3/4 with 1/4/8/16-lanes, and PCIe Gen 5 with 1/4/8-lanes when using the AMD Integrated Block for PCI Express. PCIe Gen 5x8 can be established as two links (x8/x8) to achieve the aggregate bandwidth of a 16 lane connection.

2.4.2 Installation Instructions

Follow host server user guides and installation instructions. The steps below are a general guide, and should be superseded by host system instructions.

A 16-lane physical PCIe slot is required for mechanical compatibility.

The card is also designed to use the extra mechanical retention mechanisms defined in the PCIe specification. This includes both the board keep-out region along the top edge, and the full-length handle support. It is recommended to use all board retention features supported by the host systems. These cards are heavy and can be damaged when used in systems that do not mechanically support the hardware properly. The following instructions use each retention method. If a system lacks a particular retention mechanism, the user must skip that step and understand the risk of mechanical damage is higher than if the clips were included.

This equipment is not suitable for use in locations where children are likely to be present.

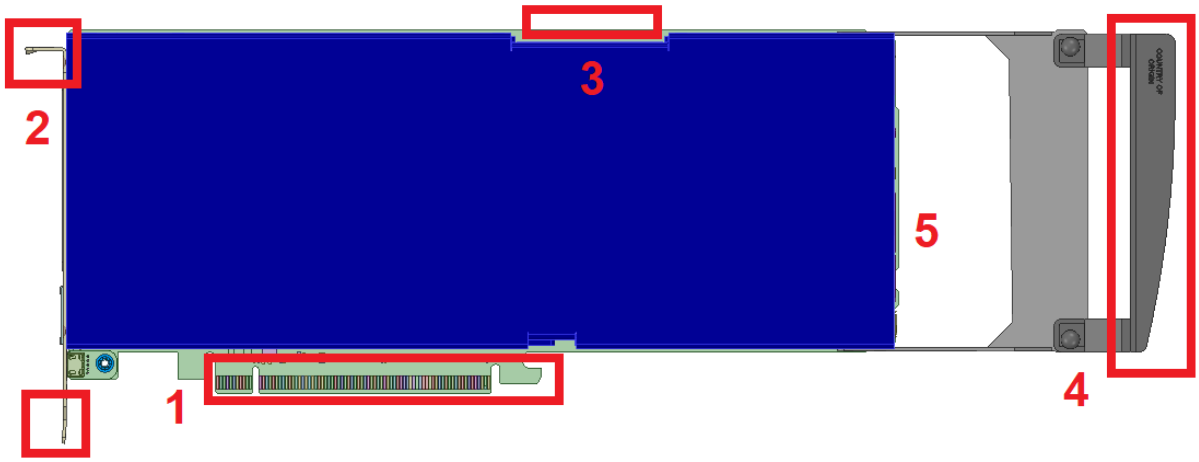


Figure 3 : Installation Steps

Installation Instructions

1 Ensure system power is off. Then hold the PCIe card securely above the PCIe slot in the system and push it straight into the connector. If the card is going onto a riser card, the riser card will need to be removed first.

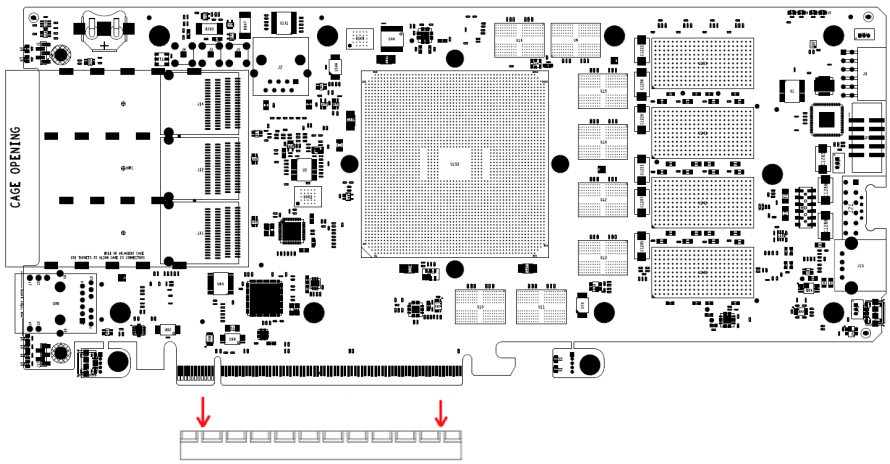


Figure 4 : Step 1) Plug In Card

2 Use the system screws or clip mechanism to secure the top of the front bracket at both hole positions.

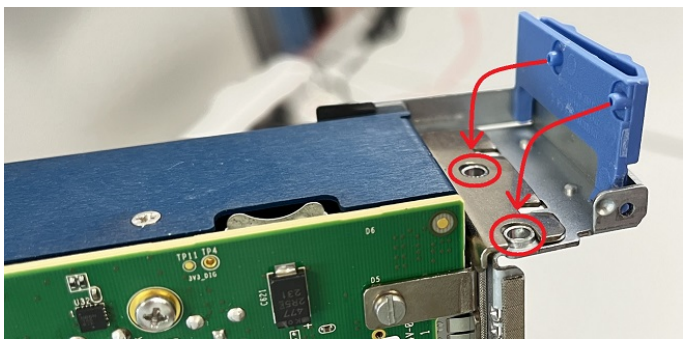


Figure 5 : Step 2) Secure Front Panel

3 Engage any system clips along the north edge to help secure the card.

4 Engage any system clips along the rear edge to help secure the card. You might need to remove the plastic handle to enable the clip to engage fully.

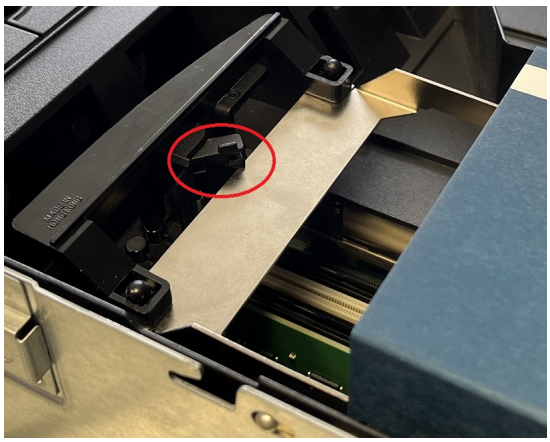


Figure 6 : Step 3+4) Secure System Clips, Collision

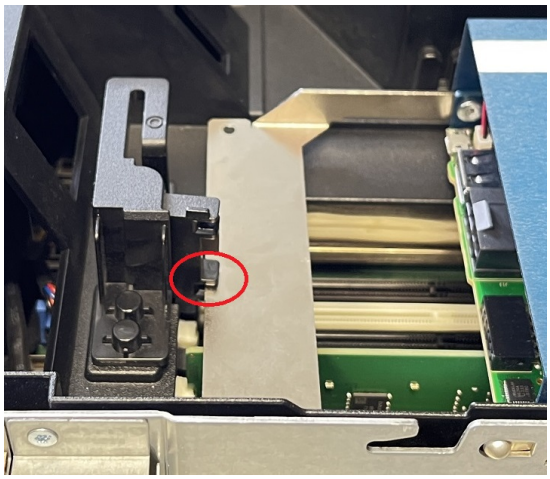


Figure 7 : Step 3+4) Secure System Clips, Correct

5 After the card has been installed and secured, the 12-pin ATX PCIe connector can be installed. This is required for all applications. This is a new power interface introduced in the PCIe Gen5 CEM specification. An adaptor cable is supplied with the ADM-PB125 to convert legacy power inputs (8-pin ATX) to this new standard. If using the adaptor cable ensure at least two of the 8-pin inputs are powered.

2.4.3 Power Requirements

The ADM-PB125 draws power from the 12-pin ATX power connector. The ADM-PB125 does not use or require the 3.3V power from the PCIe Edge (though it does use 3.3V AUX).

Power consumption estimation requires the use of the AMD PDM tool spreadsheet (https://www.amd.com/en/products/software/adaptive-socs-and-fpgas/power-design-manager.html) and a power estimator tool available from Alpha Data. Please contact **support@alpha-data.com** to obtain this tool.

The power available to the rails calculated using PDM are as follows:

Voltage	Source Name	Current Capability
0.8	VCCINT + VCCINT_GT + VCC_IO + VCC_RAM + VCC_SOC	200A
0.88	VCC_PMC + VCC_PSFP + VCC_PSLP + VCCINT_CPM5	20A
0.92	MGTYPAVCC + MGTMAVCC	20A
1.1	VCCO 1.1V	20A
1.2	MGTYPAVTT + MGTMAVTT	20A
1.5	MGTYPVCCAUX + MGTMVCCAUX	1A
1.5	VCCAUX + VCCAUX_PMC + VCCAUX_SMON	20A
1.8	VCCO_500 + VCCO_501 + VCCO 1.8V	1A
3.3	VCCO_503 + VCCO_502 + VCC0 3.3V + QSFP	20A
5V	USB-A	0.5A

Table 3 : Available Power By Rail

2.5 Thermal Performance

If the ACAP core temperature exceeds 105 degrees Celsius, the ACAP design will be cleared to protect the ADM-PB125.

The ADM-PB125 comes with a heat sink to avoid thermal overstress of ACAP, since it is typically the hottest point on the card. The ACAP die temperature must remain under 100 degrees Celsius. To estimate the ACAP die temperature: first take your total board power (see next paragraph), then multiply by Theta JA from the graph below, and add the resulting temperature to your system's internal ambient temperature.

The power dissipation can be estimated by using the Alpha Data power estimator in conjunction with the AMD Power Design Manager (PDM) downloadable at https://www.amd.com/en/products/software/adaptive-socs-and-fpgas/power-design-manager.html.

Figure 8 : System level thermal resistance (Simulated Result)

Power Estimation

- Download the Versal XPE or PDM tool.
- Set the device according to your part number details: Versal Premium Series, XCVP2502, VSVB3340 package, -2MSE/-3HSE speed grade, extended.
- Set the ambient temperature to your system ambient
- Select 'user override' for the effective theta JA. Then enter the figure associated with your system LFM in the blank field.
- Proceed to enter all applicable design elements and utilization in the following spreadsheet tabs
- Next acquire the PB125 power estimator from Alpha Data by contacting **support@alpha-data.com**.
- Enter the power figures from XPE, QSFP-DD (if used), and DRAM utilization into the Alpha Data spreadsheet to get a complete board-level estimate.

2.6 Customizations

Alpha Data provides extensive customization options for existing commercial off-the-shelf (COTS) products. Some options include, but are not limited to: custom front panel interfaces, additional networking cages in adjacent slots, enhanced heat sinks, baffles, and circuit additions.

Please contact **sales@alpha-data.com** to get a quote and start your project today.

3 Functional Description

3.1 Overview

The ADM-PB125 is a high-performance reconfigurable computing card featuring the latest AMD Adaptive Compute Acceleration Platform (ACAP) platform with the Versal XCVP2502, three QSFP-DD interfaces, PCIe Gen4x16 or 2xGen5x8, four banks of 8GB LPDDR4 each 64 bits wide, GEM0 Ethernet, QSPI, uSD, USB, UART, a Digilent PMOD site, flexible front panel I/O (RS485 for ToD, 1PPS, 10MHz, and general purpose I/O), and a robust system monitor.

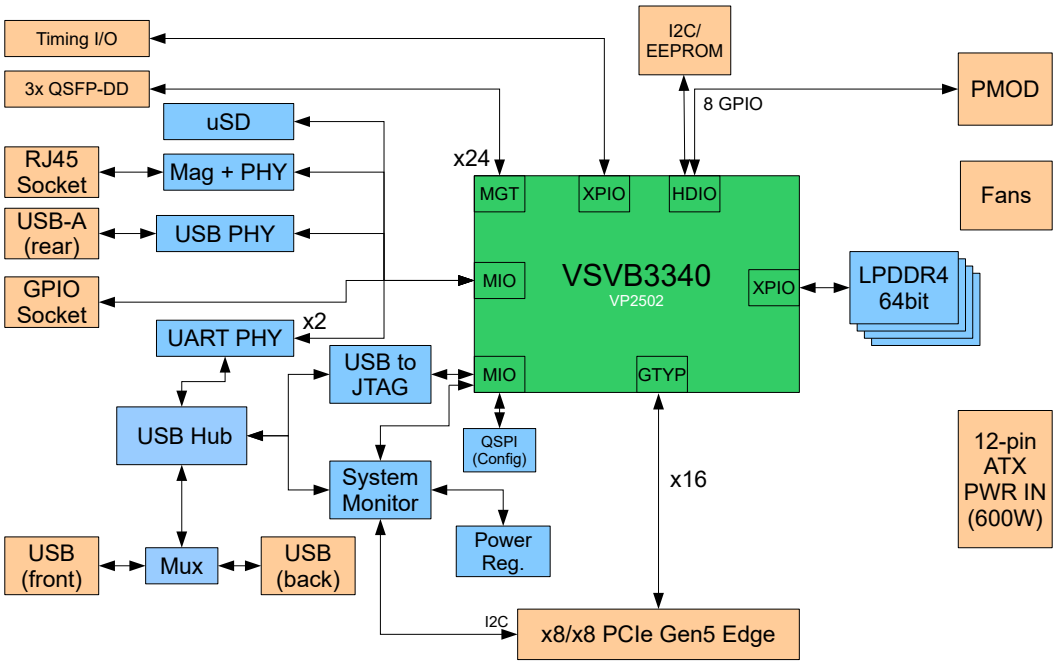


Figure 9 : ADM-PB125 Block Diagram

3.1.1 Switches

The ADM-PB125 has two octal DIP switches SW1 and SW2, located on the rear side of the board. The function of each switch is detailed below:

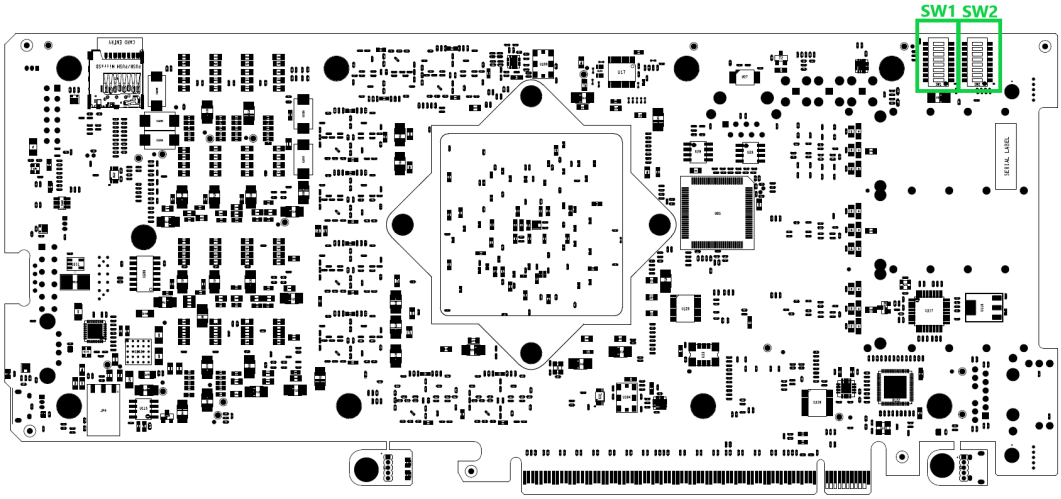


Figure 10 : Switches

Switch	Factory Default	Function	OFF State	ON State
SW1-1	OFF	Reserved	TBD	TBD
SW1-2	OFF	SI5402_I2C Isolate	Connect Si5402 I2C to PL	Isolate Si5402 I2C from PL
SW1-3	OFF	HOST_I2C_EN	System Monitor connected to PCIe slot I2C	System Monitor isolated from PCIe slot I2C
SW1-4	OFF	Service Mode	System Monitor normal operation	System Monitor Service Mode (firmware update etc.)
SW1-5	OFF	PERST to POR_B	PCIE RESET isolated from POR_B	PCIE RESET will drive POR_B low
SW1-6	OFF	POR_B	ACAP power on reset released	ACAP power on reset active
SW1-7	OFF	USER_SW0	Connected to the VP2502 at Pin BK58 (IO_L24P_GC_XCC_N8P0_712) for user applications.	
SW1-7	OFF	USER_SW1	Connected to the VP2502 at Pin A22 (LPD_MIO19_502) and is provided for user applications.	
SW2-1	ON	BootMode 0	See Table 10	
SW2-2	OFF	BootMode 1	See Table 10	
SW2-3	OFF	BootMode 2	See Table 10	
SW2-4	OFF	BootMode 3	See Table 10	
SW2-5	OFF	Reserved	TBD	TBD
SW2-6	OFF	Reserved	TBD	TBD
SW2-7	OFF	Power Off	Board will power up	Immediately power down

Table 4 : Switch Functions (continued on next page)

Switch	Factory Default	Function	OFF State	ON State
SW2-8	OFF	PMBus	PMBus accessible through ATXMEGA128	PMBus accessible through connector JP4

Table 4 : Switch Functions

3.1.2 LEDs

There are 10 LEDs on the ADM-PB125, 6 of which are general purpose and whose meaning can be defined by the user. The other 4 have fixed functions described below:

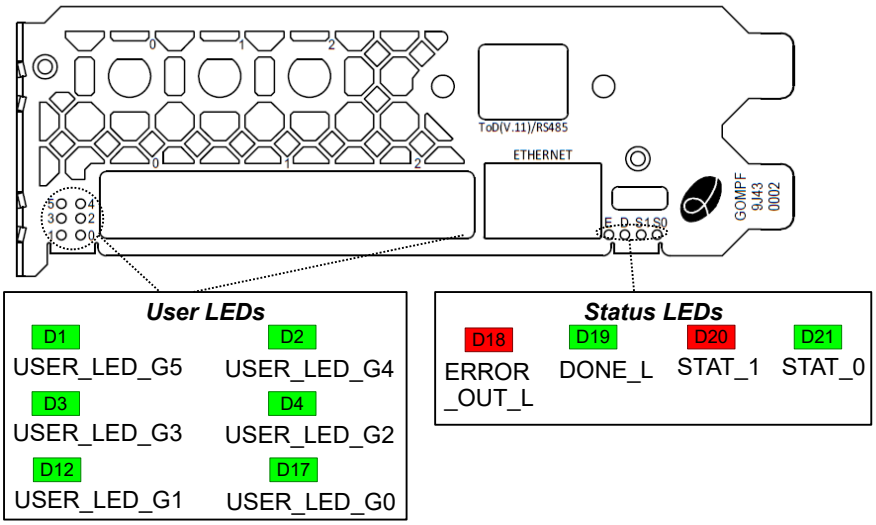


Figure 11 : Front Panel LEDs

Comp. Ref.	Function/Net Name	ON State	OFF State
D17	USER_LED_G0	User-defined '0'	User-defined '1'
D12	USER_LED_G1	User-defined '0'	User-defined '1'
D4	USER_LED_G2	User-defined '0'	User-defined '1'
D3	USER_LED_G3	User-defined '0'	User-defined '1'
D2	USER_LED_G4	User-defined '0'	User-defined '1'
D1	USER_LED_G5	User-defined '0'	User-defined '1'
D18	ERROR_OUT_L	Boot error	No error reported
D19	DONE_L	PL is configured	PL is not configured
D20	Status 1	See Status LED Definitions	
D21	Status 0	See Status LED Definitions	

Table 5 : LED Details

See Section Complete Pinout Table for full list of user controlled LED nets and pins

3.2 Clocking

The ADM-PB125 provides flexible reference clock solutions for the many multi-gigabit transceiver quads, LPDDR4 banks, and PL fabric. The reprogrammable clocks from the LMK61E2 are reconfigurable from the front panel Micro USB Interface by using Alpha Data's avr2util utility. This allows the user to configure almost any arbitrary clock frequency during application run time. The maximum clock frequency for the LMK61e2 is 900MHz. Customers who purchase RD-PB125 also have the option of embedding IP into their ACAP design that permits programmable clock reconfiguration via PCIe or from within the ACAP.

There is one Si5344 jitter attenuator. This can provide clean and synchronous clocks to the QSFP-DD quad locations at many clock frequencies. The Si5344 can be reconfigured over I2C using a controller embedded in the FPGA design.

There is one Si5402 Network Synchronizer. This can provide synchronous clocks for 5G, SyncE, and IEEE 1588 applications with 10Mhz and 1PPS inputs. The Si5402 can be reconfigured over I2C using a controller embedded in the FPGA design. Using this chip requires support directly from Skyworks. Alpha Data does not support application software for this device.

All clock names in the section below can be found in Complete Pinout Table.

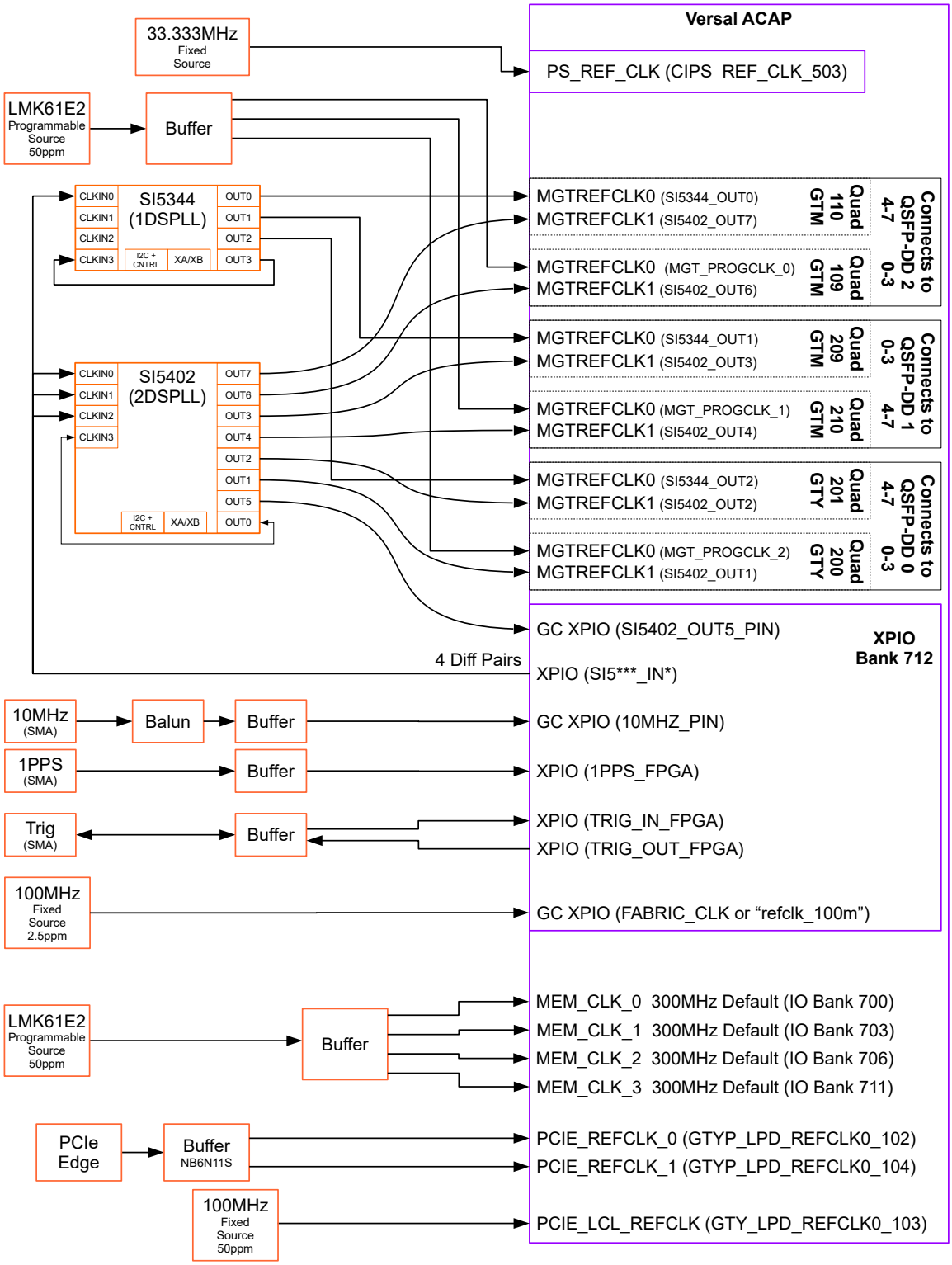


Figure 12 : Clock Topology

3.2.1 LMK61E2

The ADM-PB125 uses the LMK61E2 for arbitrary clock frequency synthesis. For complete technical details, please reference the datasheet:
https://www.ti.com/lit/ds/symlink/lmk61e2.pdf

The ADM-PB125 uses two LMK61E2 devices in the clock architecture. These can be accessed through either the USB or PCIe link using the AVR2UTIL application. See additional details on avr2util in the section: Micro USB Interface.

To re-program the LMK61E2 in a non-volatile manner, issue the following command:

```
avr2util <other options> setclknv-regmap <clock#> <reg. map file>
```

> **Note:**
> Each LMK61E2 is rated for only 100 non-volatile write operations.

To re-program the LMK61E2 in a volatile manner, issue the following command:

```
avr2util <other options> setclk-regmap <clock#> <reg. map file>
```

<other options> should be left blank for PCIE, and '-usbcom' for USB.

<clock#> is 0 for MGT_PROGCLK and 1 for MEM_CLK.

<reg. map file> is a text file generated using the "LMK61xx Oscillator Programming Tool — SNAC074.ZIP" which can be obtained with a TI login from this page: https://www.ti.com/tool/LMK61E2EVM. After you have the tool installed, launch the application, type in the desired frequency, select "LVDS" output standard, click "Generate Configuration", then go to "File->Export hex register values"

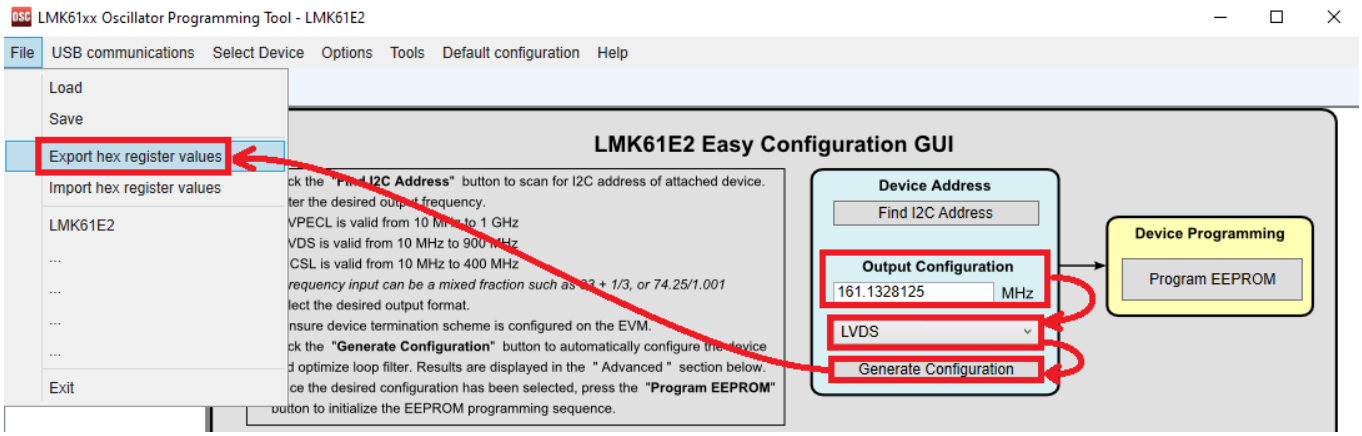


Figure 13 : LMK61xx Oscillator Programming Tool GUI

3.2.2 Si5344

If jitter attenuation is required please see the SI5344 datasheet.

The SI5344 is pre-configured to expect 322.265625MHz on IN0, and will output 161.1328125MHz on all outputs. The non-volatile memory on the device can be changed one more time. For details on burning the non-volatile memory, see section “4.3 NVM Programming” of the SI5344 Reference Manual.

There is one input clock that originates in the ACAP PL (board net name SI5344_IN0_P/N). This allows the application design to feed the clock from anywhere within the ACAP PL.

Three output clocks are connected to quads 110, 201, and 209 to provide clocking capability for each QSFP-DD interface.

The LOL signals for the Si5344 are available for use, and can be located at net names SI5344_LOL_XAXB_1V5_N and SI5344_LOL_1V5_N in the Complete Pinout Table.

The active low reset of the Si5344 is accessible to the ACAP. See net names SI5344_RST_1V5_N in the Complete Pinout Table.

Note:
Each sideband signal has an external pull-up resistor.

The Si5344 configuration register map is volatile unless burned into NVM. You are only allowed to burn a register map twice during the product's lifetime, and Alpha Data has used one of these already. To write the register map use nets SI5344_SDA_1V5 and SI5344_SCL_1V5 at pins located in the Complete Pinout Table. The Si5344 device is configured using the I2C address shown in the table below:

device	7bit Hex Address	Binary Address
Si5344	68	110_1000

Table 6 : Si5344 address table

3.2.3 Si5402

If a Network Synchronizer Clock for 5G/SyncE/IEEE 1588 applications is required please see the reference documentation for the Si5402.
https://www.skyworksinc.com/en/Products/Timing/NetSync-Network-Synchronizer-Clocks/Si5402A

There are three input clocks that originate in the ACAP PL (board net name SI5402_IN*_P/N). This allows the application design to feed the clock from anywhere within the ACAP PL and forward 10MHz and 1PPs signals.

Six output clocks are connected to quads 200, 201, 209, 210, 109, and 110 to provide clocking capability for each QSFP-DD interface.

The GPIO signals for the Si5402 are available for use and can be located at net names SI5402_GPIO* in the Complete Pinout Table.

The active low reset of the Si5402 is accessible to the ACAP. See net names SI5402_RST_1V5_N in the Complete Pinout Table.

Note:
Each sideband signal has an external pull-up resistor.

The Si5344 configuration register map is volatile. To write the register map use nets SI5402_1V5_SDA and SI5402_1V5_SCL at pins located in the Complete Pinout Table. The Si5402 device is configured using the I2C address shown in the table below:

device	7bit Hex Address	Binary Address
Si5344	58	101_1000

Table 7 : Si5402 address table

3.2.4 PCIe Reference Clocks

The 16 MGT lanes connected to the PCIe card edge use MGT tiles 102 through 105 and use the host system's 100 MHz PCIe reference clock (net name PCIE_REFCLK_0_P/N or PCIE_REFCLK_1_P/N in the Complete Pinout Table).

Alternatively, a more stable but asynchronous onboard 100MHz clock is available as well (net name PCIE_LCL_REFCLK_P/N in the Complete Pinout Table).

3.2.5 Fabric Clock

The design offers a fabric clock (net name FABRIC_CLK_P/N) which is a high accuracy 2.5ppm 100 MHz clock. This clock is intended to be used for the PL designs. The fabric clock is connected to a Global Clock (GC) pin.

Use constraints IOSTANDARD LVCMOS15 for this reference clock.

See net names FABRIC_CLK_1V5 in the Complete Pinout Table for pin locations.

In the Alpha Data provided board file, this is called "refclk_100m"

3.2.6 PS Reference Clock (PS_REF_CLK)

A 33.333MHz clock is fed into the dedicated REF_CLK_503 pin to drive the processor system. This clock has an accuracy tolerance of 50ppm.

3.2.7 MGT Programmable Clock

The MGT reference clock connects to one quad of each QSFP-DD connector. This programable clock has a default 161.1328125MHz reference clock. This clock frequency can be changed to any arbitrary clock frequency up to 900MHz by re-programming the LMK61E2 reprogrammable clock oscillator. See details on avr2util in the section: Micro USB Interface.

See net names MGT_PROGCLK_*_PIN_P/N in the Complete Pinout Table for pin locations.

3.2.8 Memory Clocks

Each of the four memory banks has their own buffered 300MHz reference clock. This clock frequency can be changed to any arbitrary clock frequency up to 900MHz by re-programming the LMK61E2 reprogrammable clock oscillator. See details on avr2util in the section: Micro USB Interface.

See net names MEM_CLK_*_PIN_P/N in the Complete Pinout Table for pin locations.

See LPDDR4 SDRAM for more information on the memory banks and their physical locations.

These clocks are not fabric accessible. They are reserved for the Versal LPDDR4 cores.

3.3 PCI Express

The ADM-PB125 is capable of PCIe Gen 1/2/3/4 with 1/4/8/16 lanes and bifurcated Gen 5 with 1/4/8 lanes. The ACAP drives these lanes directly using the Integrated PCI Express block from AMD. Negotiation of PCIe link speed and number of lanes is automatic and does not require user intervention.

PCI Express reset (PERST#) is connected to the ACAP through a buffer. See Complete Pinout Table signal PERST_PL_L for fabric accessible location, and PCIE_RST_1V8_L for the PS locations.

The pin assignments for the high-speed lanes are provided in the pinout attached to the Complete Pinout Table, see net names PCIE_TX*_PIN_P/N and PCIE_RX*_P/N.

3.4 LPDDR4 SDRAM

Four banks of LPDDR4 SDRAM memory are soldered down to the board. The available density of the memory is 8GB/per bank, 32GB total. The memory interface is 64-bit wide data. The maximum signalling rate is 3933 MT/s.

Memory solutions are available from AMD (See AMD PG313 Versal ACAP Programmable Network on Chip and Integrated Memory Controller v1.0). LPDDR4_0 through 2 use the Non-Flipped Pinout, and LPDDR4_3 uses the Flipped Pinout. An example memory exerciser project is included in the RD-PB125 (Release date TBD). All pin location information is included in Complete Pinout Table and the board file.

The components used are Micron MT53E1G32D2FW-046 IT or equivalent.

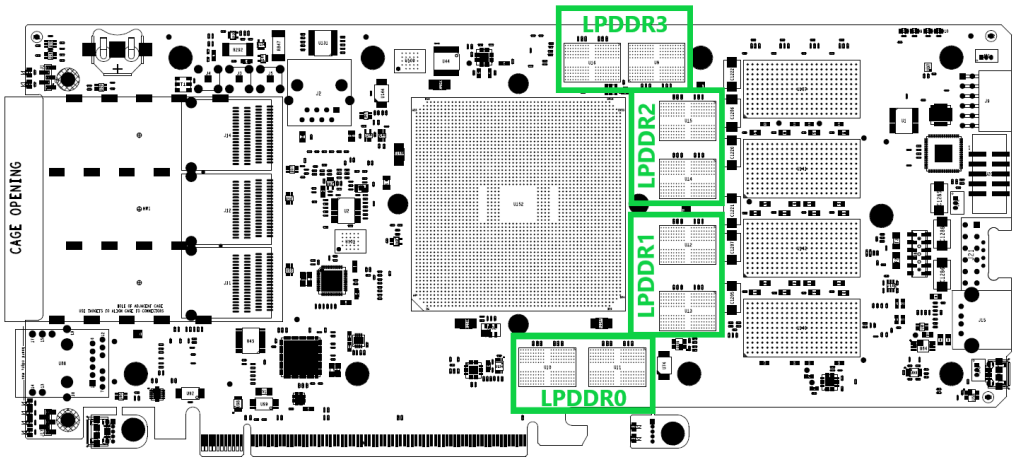


Figure 14 : LPDDR4 bank locations by index

3.5 QSFP-DD

Three QSFP-DD cages are available at the front panel. These cages are capable of housing either QSFP28 or QSFP-DD cables (backwards compatible). Both active optical and passive copper QSFP-DD/QSFP28 compatible models are fully compliant. The communication interface can run at up to 28 Gbps per channel on GTY and 56 Gbps per channel on GTM. Two cages connect to GTM transceivers and one cage connects to GTY transceivers. Each QSFP-DD cage has 8 channels. QSFP2 and QSFP1 are 56Gbps PAM4 capable as they are driven by with Xilinx GTM Transceivers. QSFP0 is ideally suited for 8x 10G/25G/50G, 2x 100G/200G, 1x400G Ethernet, or any other protocol supported by the Xilinx GTY Transceivers. Please see AMD User Guide AM002 (GTY) and AM017 (GTM) for more details on the capabilities of the transceivers.

All QSFP-DD cages have control signals connected to the FPGA. Their connectivity is detailed in the Complete Pinout Table at the end of this document. The notation used in the pin assignments is QSFP0*, QSFP1*, and QSFP2*, with locations clarified in the diagram below.

The Management Interface of each QSFP-DD cage is connected to the ACAP, as detailed in Complete Pinout Table. The available signals are SDA/SCL (I2C), INT_L (interrupt), LPMODE (low power mode), RST_L (reset), and MODPRS_L (module present).

Note:
The LPMODE (Low Power Mode) to the cage is pulled down by default.

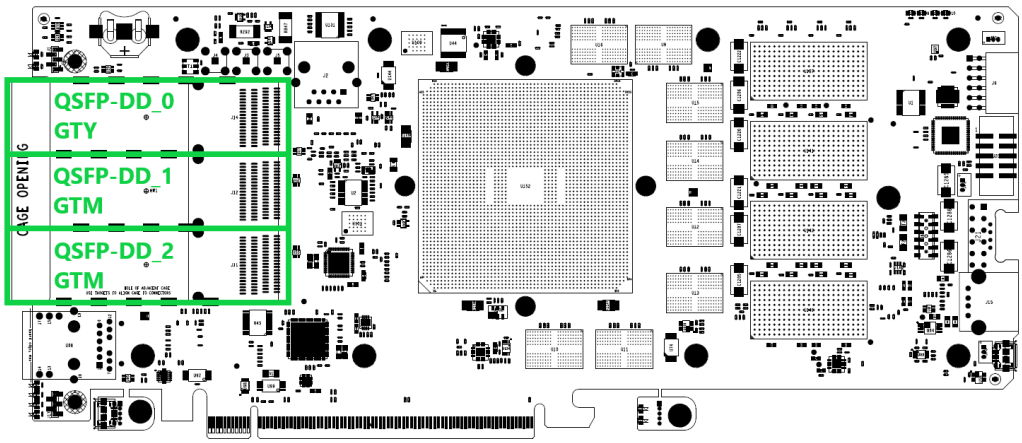


Figure 15 : QSFP-DD Location

3.6 Front I/O timing inputs

The ADM-PB125 includes several timing and signal inputs that are critical for high-performance synchronous networking. This section details the four available timing inputs.

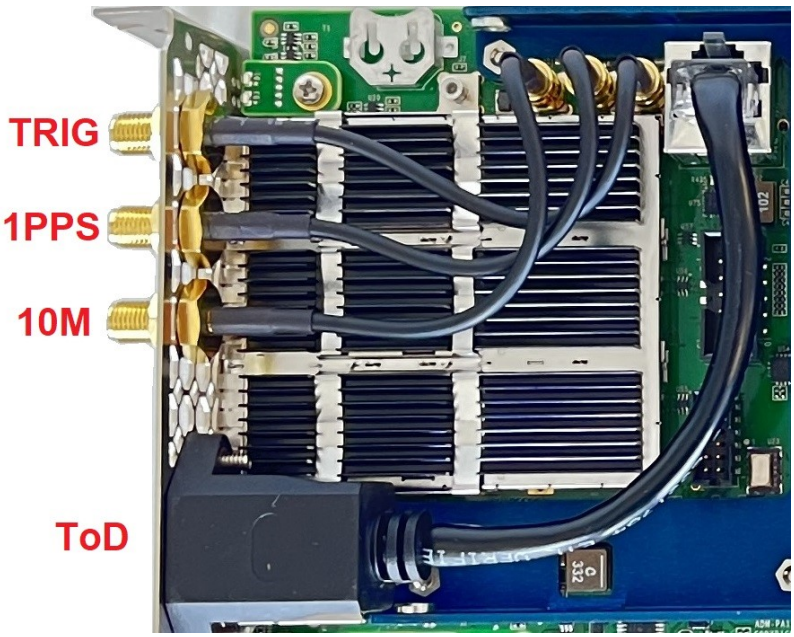


Figure 16 : Front I/O timing inputs

3.6.1 Trigger Input/Output (I/O)

One of the SMA connectors is used for a general purpose I/O. This signal can be driven as an output or received as an input.

A small '0' is printed on the faceplate at the TRIG I/O connector.

The input receiver is always active. The output driver buffers net "TRIG_OUT" onto the SMA connector when net "TRIG_OUT_EN" is driven low.

The trigger input is designed for unbalanced 50-ohm input signal at either 5V or 1.8V signal levels. The port is configured as an input when both nets "TRIG_TE_EN" and "TRIG_OUT_EN" are driven high. "TRIG_TE_EN" actives a 50-ohm load to GND. "TRIG_OUT_EN" is an active low control signal that disables the output driver when driven high.

The buffers used are low latency (less than 5ns), and the full schematic detail is shown below:

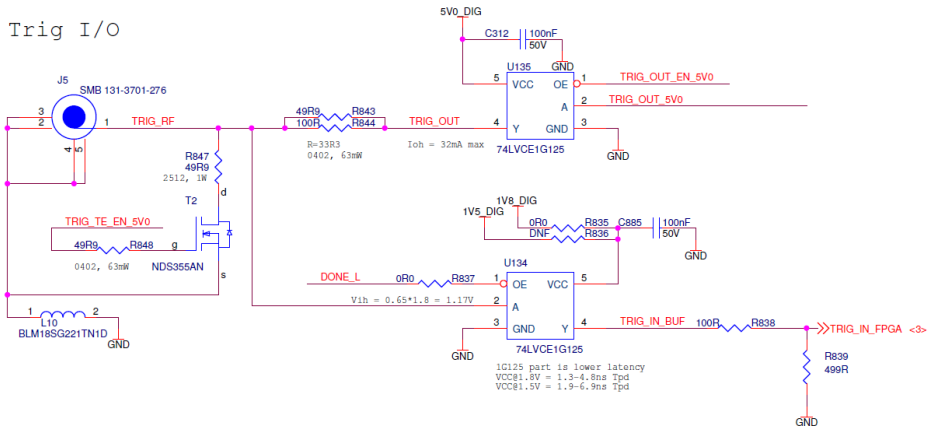


Figure 17 : Trig Schematic

3.6.2 1PPS Input

One of the SMA connectors is used for a 1PPS input. This is a general input that can be used for many unbalanced 50-ohm input signal up to 5V in amplitude.

A small '1' is printed on the faceplate of the 1PPS input connector.

The buffers used are low latency (less than 5ns), and the full schematic detail is shown below:

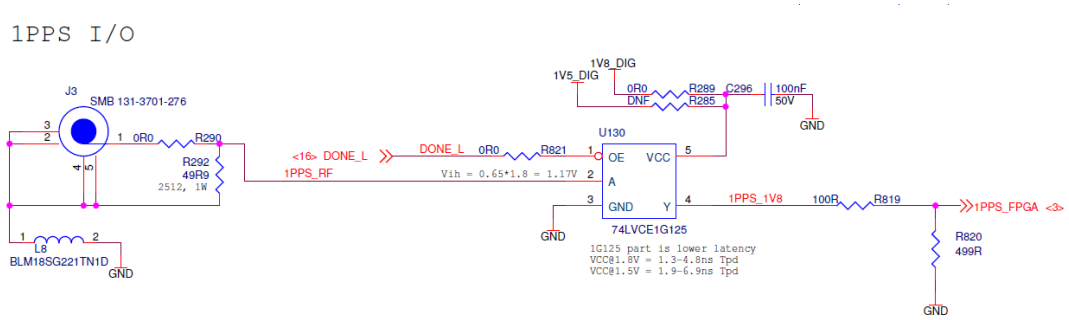


Figure 18 : 1PPS Input Schematic

3.6.3 10MHz Input

One of the SMA connectors is used for a 10MHz input. This is a specific input that has a narrow frequency band around 10MHz and expects 0.5V to 5V peak-to-peak input voltage.

A small '2' is printed on the faceplate at the 10MHz input connector.

The signal passes through a balun and LVDS buffer before entering the ACAP. The full schematic detail is shown below:

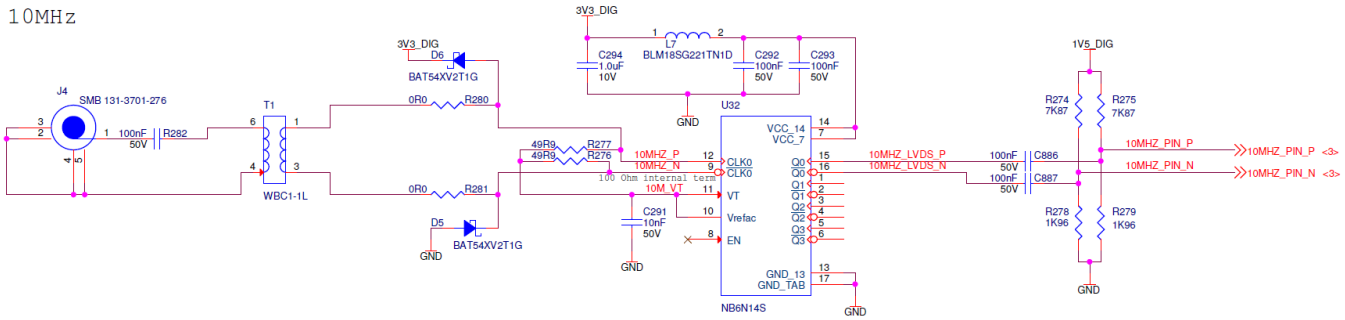


Figure 19 : 10MHz Input Schematic

3.6.4 Time of Day (ToD) / One Pulse per Second (1PPS)

One of the RJ45 jacks at the front panel is for Time of Day (ToD) or generic RS485 input/output. The port is labeled on the front panel for clarity.

Net "485_*_DE/RE_L_FPGA" is used to control the direction of this interface. By default, the DE/RE_L pins are pull-down, so the RS485 drivers are set as inputs to the ACAP. If either DE/RE_L pins are driven high, the RS485 transceivers will become outputs respectively.

The transceivers are low latency (18.5ns ±3.5ns), and the full schematic detail is shown below:

TOD + 1PPS

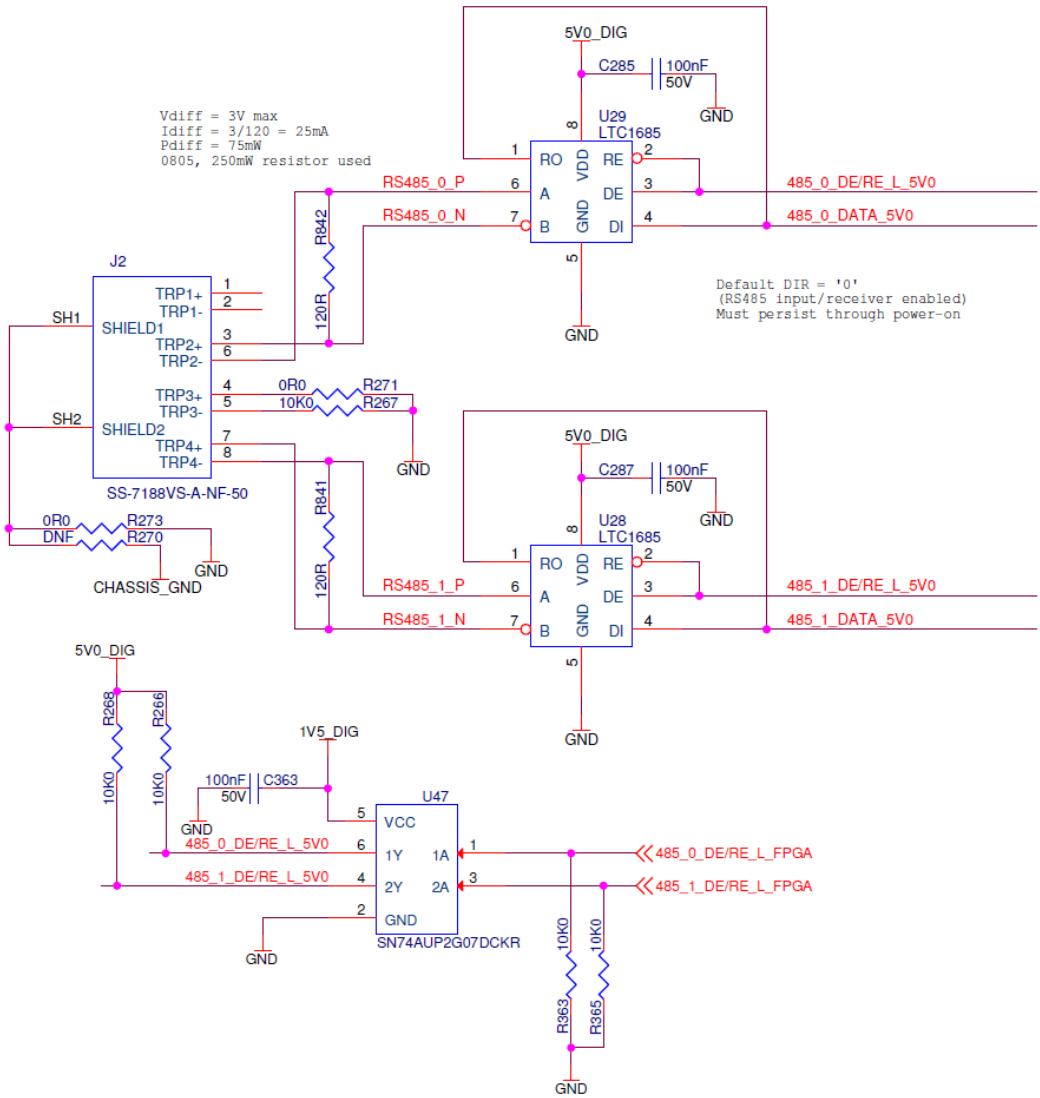


Figure 20 : ToD/1PPS or RS485 Schematic

3.7 System Monitor

The ADM-PB125 monitors select temperatures, voltages, and currents in order to provide an indication of board health. The monitoring is implemented using an AVR microcontroller. This information can be read out via USB using the avr2util utility. Alternatively, the sensor information can be read directly by the ACAP or via PCIe if RD-PB125 is purchased (reference design package).

If the core ACAP temperature exceeds 105 degrees Celsius, the ACAP image will be cleared to prevent damage to the card.

Monitors	Identifier	Purpose/Description
ETC	ETC	Elapsed time counter (seconds)
EC	EC	Event counter (power cycles)
12V_AUX	ADC00	12V board input voltage from 12-pin ATX cable
12V_AUX_I	ADC01	12V board input current from 12-pin ATX cable in amps
1V8_DIG	ADC02	1.8V generated onboard for the ACAP
1V0_DIG	ADC02	1.0V generated onboard for the ACAP
3V3_AUX	ADC04	3.3V auxiliary board input supply from PCIE edge
3V3_DIG	ADC05	3.3V generated onboard for QSFP-DD and other circuits
1V8_SI5402	ADC06	1.8V generated onboard for Si5402
1V5_DIG	ADC07	1.5V generated onboard for ACAP IO voltage (VCCO)
1V5_AVCCAUX	ADC08	1.5V generated onboard for ACAP Aux voltage
1V2_AVTT	ADC09	1.2V generated onboard for transceiver Power (AVTT)
1V1_DIG	ADC10	1.1V generated onboard for LPDDR4 SDRAM and ACAP (VCCO)
0V92_AVCC	ADC11	0.88V generated onboard for transceiver Power (AVCC)
VCC_PMC	ADC12	0.88V generated onboard for ACAP core
VCC_INT	ADC12	0.8V generated onboard for ACAP core
uC_Temp	TMP00	uC on-die temperature
Board0_Temp	TMP01	Board temperature at U58
Board1_Temp	TMP02	Board temperature at U80
ACAP_Temp	TMP03	ACAP underside temperature

Table 8 : Voltage, Current, and Temperature Monitors

3.7.1 System Monitor Status LEDs

LEDs D20 (Red) and D21 (Green) indicate the card health status.

LEDs	*Status*
Green	Running and no alarms
Green + Red	Standby (Powered off)
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Green + Flashing Red (alternating)	Service Mode
Flashing Green + Red	Attention - alarm active
Red	Missing application firmware or invalid firmware
Flashing Red	ACAP configuration cleared to protect board

Table 9 : Status LED Definitions

3.8 Micro USB Interface

The ACAP can be configured directly from the USB connection on either the front panel or the rear card edge. The ADM-PB125 utilizes the Digilent USB-JTAG converter which is supported by the AMD software tool suite. Simply connect a micro-USB AB-type cable between the ADM-PB125 USB port and a host computer with Vivado installed. Vivado Hardware Manager will automatically recognize the ACAP and allow you to configure the ACAP and the SPI configuration Flash memory.

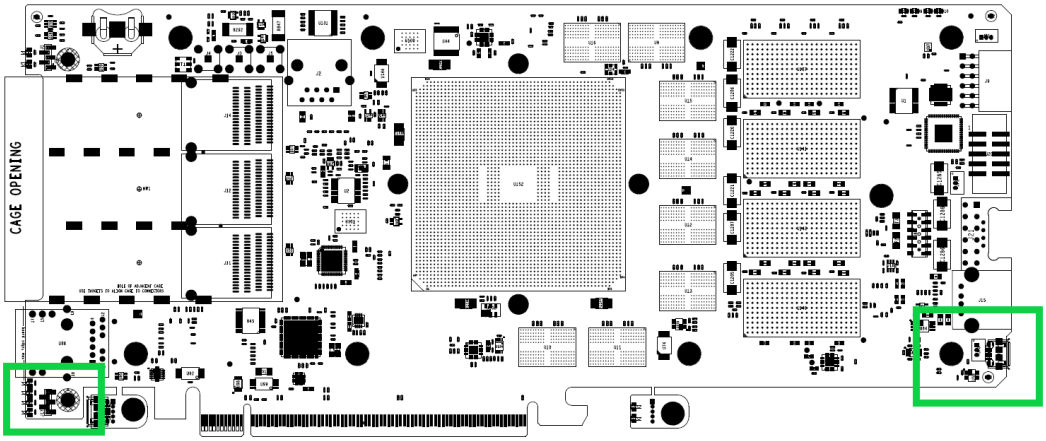


Figure 21 : USB Location

The same USB connector is used to directly access the system monitor system. All voltages, currents, temperatures, and non-volatile clock configuration settings can be accessed using Alpha Data's avr2util software at this interface.

Avr2util for Windows and the associated USB driver is downloadable here:
https://support.alpha-data.com/pub/firmware/utilities/windows/

Avr2util for Linux is downloadable here:
https://support.alpha-data.com/pub/firmware/utilities/linux/

Use this command to see all options:

```
avr2util.exe /?
```

Use this command to display all sensor values:

```
avr2util.exe /usbcom \\.\com4 display-sensors
```

Here is an example of changing the MGT_PROGCLK to 156.25MHz immediately:

```
avr2util.exe /usbcom \\.\com4 setclk-regmap 0 lmk61e2_lvds_156250000.txt
```

To generate the register text file, please reference LMK61E2.

Setclk index 0 = MGT_PROGCLK and index 1 = MEM_CLK.

Here is an example of changing the boot mode from uSD to QSPI on the next power-up event:

```
avr2util.exe /usbcom \\.\com4 set-boot-mode qspi24
```

Boot-mode commands use open drain drivers and can only drive mode pins low.

In the examples above, change 'com4' to match the com port number assigned under Windows Device Manager.

3.9 Configuration

There are three main ways of configuring the ACAP on the ADM-PB125:

- From QSPI Flash memory, at power-on, as described in Section 3.9.1
- From uSD Flash memory, at power-on, as described in Section 3.9.2
- Using USB cable connected at either USB port as described in Section 3.9.3

3.9.1 Configuration From QSPI Flash Memory

The ACAP can be automatically configured at power-on from two 1 Gbit QSPI flash memory devices configured as an x8 dual parallel SPI device (2x Micron part number MT25QU02GCBB8E12).

The ADM-PB125 is shipped with a simple "hello world" application loaded into QSPI. On request, Alpha Data can pre-load custom bitstreams during the production test. Please contact **sales@alpha-data.com** in order to discuss this possibility.

At power-on, the ACAP attempts to configure itself automatically according to the mode pins as described in Section 3.9.4. If the mode is set to QSPI24 or QSPI32, the ACAP will search on the header of the binary that has been flashed into the card. This normally results in SPIx8 configuration.

The Alpha Data System Monitor is also capable of reconfiguring the flash memory and reprogramming the ACAP. This provides a useful failsafe mechanism to re-program the ACAP even if it drops off the PCIe bus. The system monitor can be accessed with avr2util over USB at the front panel and rear edge.

3.9.2 Configuration From uSD Flash Memory

The ACAP can be automatically configured at power-on from the Micro Secure Digital card (uSD) slot along the north edge of the card.

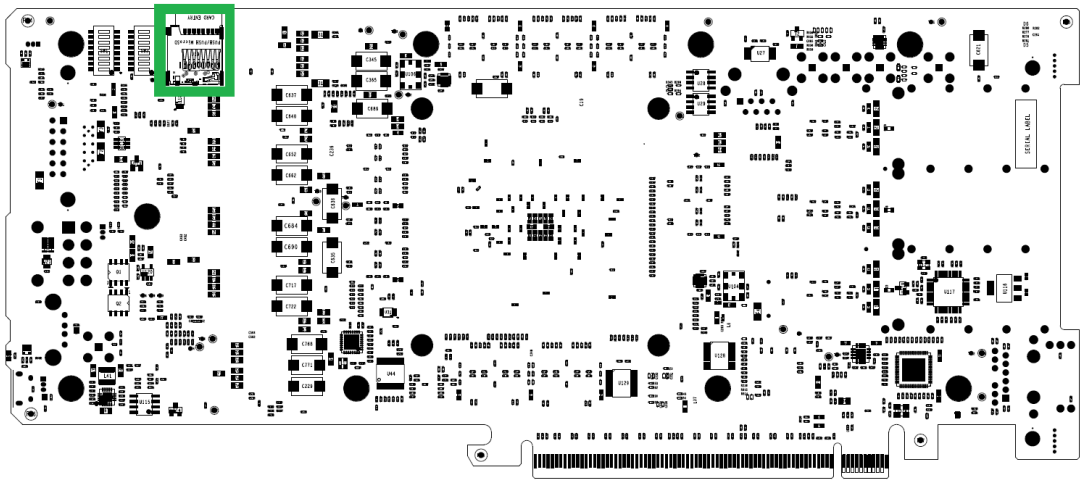


Figure 22 : uSD Location

The ADM-PB125 is shipped with a simple PCIe endpoint bitstream which should be visible to the operating system (using Windows Device Manager or “lspci” in Linux) in order to provide confidence that the card is working correctly when installed in a system. On request, Alpha Data can pre-load custom bitstreams during the production test. Please contact **sales@alpha-data.com** in order to discuss this possibility.

At power-on, the ACAP attempts to configure itself automatically according to the mode pins as described in Section 3.9.4. Alpha Data ships these cards set to the uSD boot mode by default.

3.9.3 Configuration via JTAG

A micro-USB AB Cable may be attached to the front panel or rear edge USB port. This permits the ACAP to be reconfigured using the AMD Vivado Hardware Manager and Vitis via the integrated Digilent JTAG converter box. The device will be automatically recognized in Vivado Hardware Manager and Vitis.

For more detailed instructions, please see “Using a Vivado Hardware Manager to Program an FPGA Device” section of AMD UG908

3.9.4 Boot Modes

MODE3 (SW2-4)	MODE2 (SW2-3)	MODE1 (SW2-2)	MODE0 (SW2-1)	Boot Mode
ON	ON	ON	ON	JTAG
ON	ON	ON	OFF	Quad SPI (24-bit addressing)
ON	ON	OFF	ON	Quad SPI (32-bit addressing)
OFF	OFF	OFF	ON	SD Flash - SD 3.0

Table 10 : Boot Mode Selection

Note: all other possible switch settings are reserved / invalid.

The system monitor can also control the mode pins, enabling remote changes to boot the device for golden image fallback and recovery. The system monitor can drive the MODE pins low (open drain drive), so it is recommended to leave the switches in the OFF positions or set them to SD 3.0 boot mode. From there, the user can issue commands to change the boot mode between "sd1_v3" or "qspi32" and then reboot the board:
Loading an image from qspi32 remotely:

- avr2util.exe -usbcom com4 set-boot-mode qspi32
- avr2util.exe -usbcom com4 set-brd-power off
- avr2util.exe -usbcom com4 set-brd-power on

Use set-boot-mode to immediately change boot mode settings. Use set-boot-mode-nv to change boot mode setting in a non-volatile manner after a complete system power cycle.

3.10 ULPI USB Interface

The MIO ULPI USB interface is instantiated. See MIO Map

Part number USB3320C-EZK is used for PHY electrical conversion. This PHY is capable of USB 2.0 communication speeds. An onboard supply provides 5V @ 500mA on the VBUS pin of the USB receptacle. The location of the USB PHY is located along the back edge of the card.

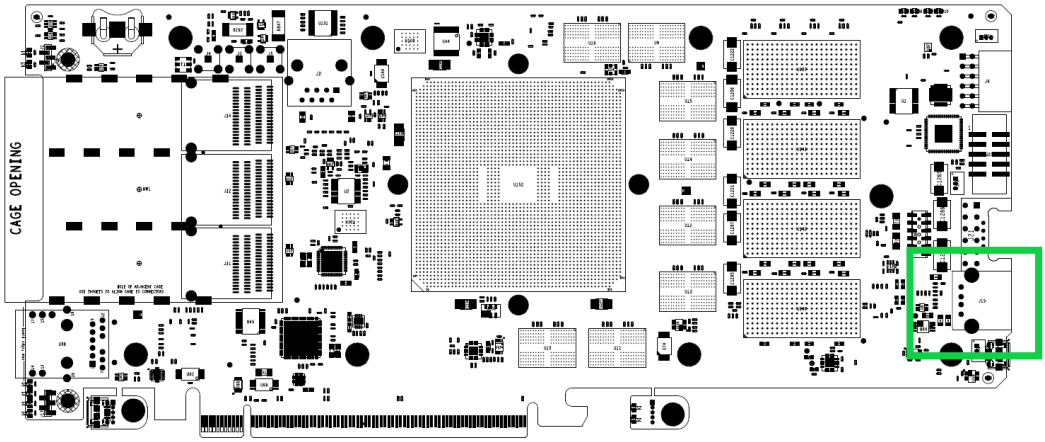


Figure 23 : ULPI USB Location

3.11 UART interfaces

UART0 and UART1 interfaces are available. See MIO Map

Both of these UART interfaces are brought out through the onboard USB hub which can be accessed at either the front or the back edge of the card.

UART0 passes through an FT230XQ USB to UART converter. This device is powered from the USB VBUS supply provided by the USB cable. This UART interface will appear in the host system as soon as the USB cable is installed, even before the ADM-PB125 is powered up. This interface is suitable for capturing power-on messages from the processor.

UART1 passes through an FT2232HQ USB to UART converter. This is the same IC that performs the USB to JTAG conversion. This UART interface will not appear in the system until after the board is fully powered and is not suitable for capturing power-on messages from the processor.

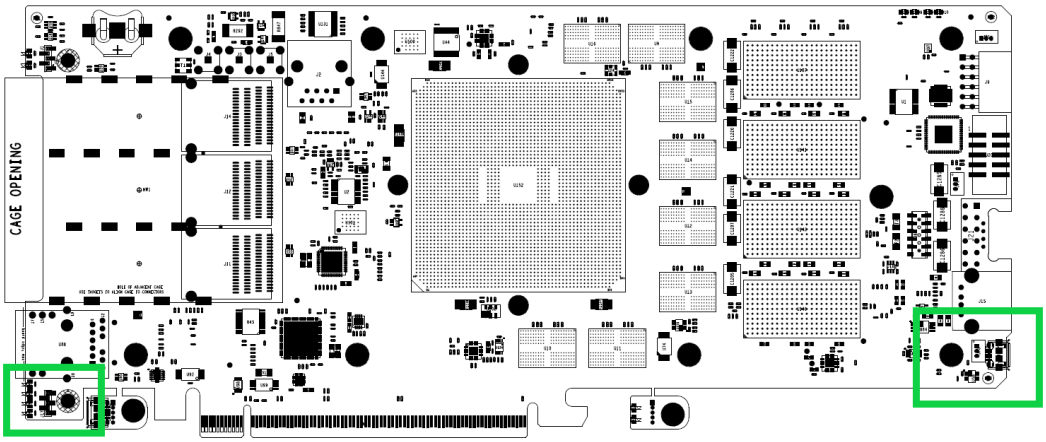


Figure 24 : USB UART Location

3.12 GEM0

The Gigabit Ethernet Manager (GEM0) is interfaced with a Microchip VSC8541 to provide 10/100/1000 Base-T Ethernet to the ACAP. This interface is accessible at the front panel.

A dedicated reset signal is connected to the MIO pins, see signal name GEM0_RST_L in Complete Pinout Table. This pin has an external pull-up and its use is optional.

See MIO Map

The Ethernet jack has two LED colors available. They are mapped to the VSC8541 PHY LED[*] pins and their function is user-defined over the GEM0_MDIO interface. The LED mapping is: green->LED[0], orange->LED[1]

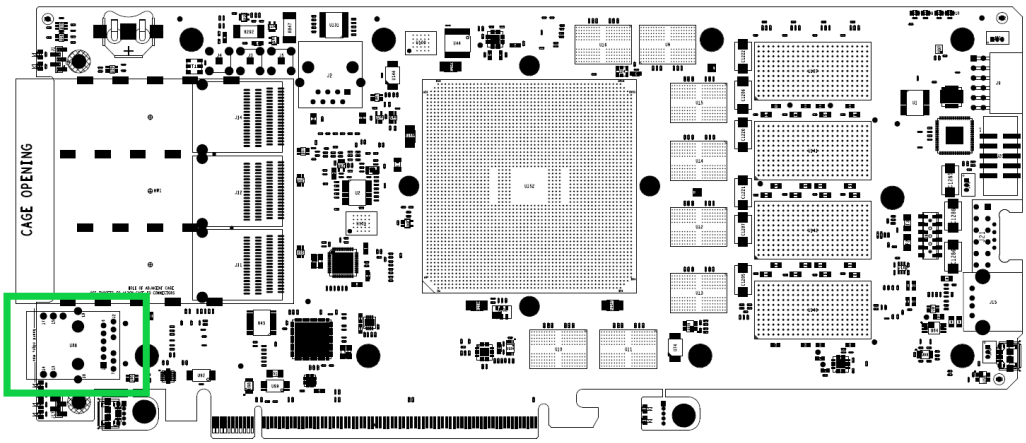


Figure 25 : GEM0 Ethernet Location

3.13 User EEPROM

A 2Kb I2C user EEPROM is provided for storing MAC addresses or other user information. The EEPROM is part number CAT34C02HU4IGT4A

The address pins A2, A1, and A0 are all strapped to a logical '0'.

Write protect (WP), Serial Clock (SCL), and Serial Data (SDA) pin assignments can be found in Complete Pinout Table with the names SPARE_WP_1V1, SI5344_SDA_1V5, and SI5344_SCL_1V5 respectively.

WP, SDA, and SCL signals all have external pull-up resistors on the card.

3.14 PMOD

The ADM-PB125 includes a twelve-pin right-angle connector PMOD host interface at the rear edge of the card with a full 0.9" clearance. This interface is connected to the PL of the ACAP.

See the PMOD Specification for full details.

Signals from this interface start with the name PMOD* and can be found in Complete Pinout Table.

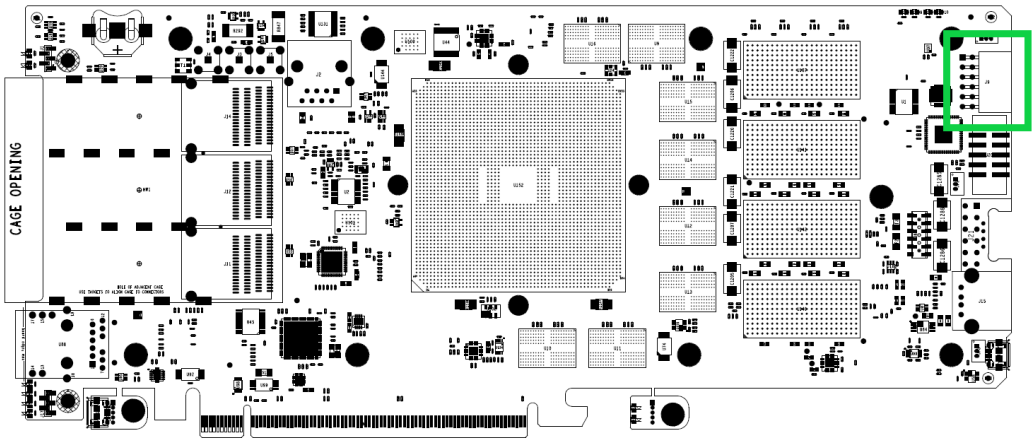


Figure 26 : PMOD location

3.15 Battery

The ADM-PB125 includes a battery cage that powers VCC_BATT (ACAP pin AG33). This cage is Keystone 3096 holder. Use with SR44 batteries with a nominal voltage of 1.55V.

The battery includes a 470uF capacitor in parallel to hold a charge during a brief battery change operation. Given a worst case VCC_BAT current of 3.5uA, the 470uF capacitor will loose about 100mV every 13 seconds.

Install the battery through the opening along the side of the stiffening plates.

A battery is not included.

The battery used must meet the following standard: IEC 60086-4 or IEC 60086-5.

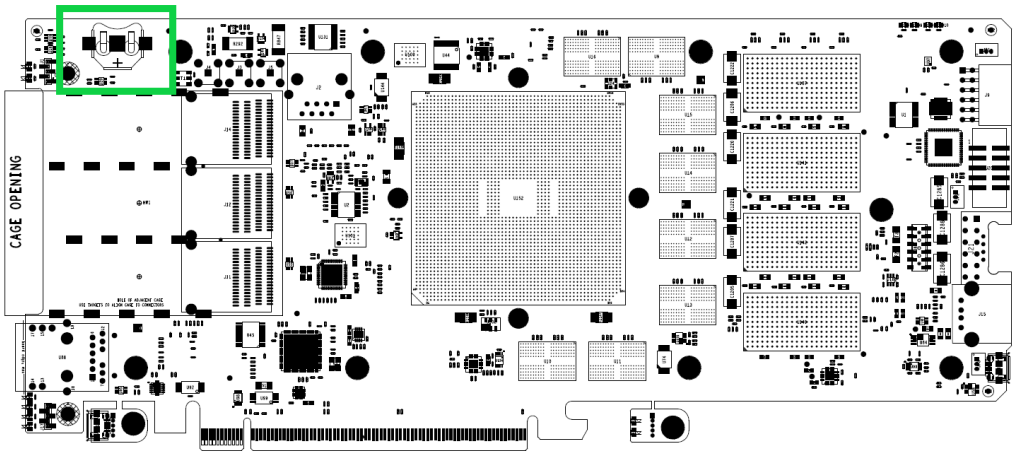


Figure 27 : Battery Location

3.16 Fan Speed Control

The ADM-PB125 uses a fan speed controller to drive and monitor the 3 built-in fans.

The fan controller is part number MAX6620ATI+

AVR2UTIL can be used to control fan speed. Reference the MAX6620 datasheet for register details.

Below are example avr2util raw i2c commands that can be used to change fan speeds using RPM mode.

Configure all fans for RPM mode:

```
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x00 0x00
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x01 0x00
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x02 0xC8
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x03 0xC8
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x04 0xC8
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x06 0x64
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x07 0x64
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x08 0x64
```

Set all fan speeds to 4K RPM:

```
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x20 0x40
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x21 0x00
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x22 0x40
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x23 0x00
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x24 0x40
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x25 0x00
```

Set all fan speeds to 10K RPM:

```
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x20 0x19
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x21 0x00
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x22 0x19
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x23 0x00
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x24 0x19
avr2util.exe /usbcom \\.\com4 i2c-write 1 0x2a 0x25 0x00
```

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Appendix A: MIO Map

Pin Number	Pin Name	Signal Name	Comment
H25	PMC_MIO0_500	qspi0_clk	Dual-Parallel Quad SPI
J25	PMC_MIO1_500	qspi0_io[1]	Dual-Parallel Quad SPI
K25	PMC_MIO2_500	qspi0_io[2]	Dual-Parallel Quad SPI
L25	PMC_MIO3_500	qspi0_io[3]	Dual-Parallel Quad SPI
N25	PMC_MIO4_500	qspi0_io[0]	Dual-Parallel Quad SPI
N24	PMC_MIO5_500	qspi0_cs_b	Dual-Parallel Quad SPI
M24	PMC_MIO6_500	NC	-
L24	PMC_MIO7_500	qspi1_cs_b	Dual-Parallel Quad SPI
K24	PMC_MIO8_500	qspi1_io[0]	Dual-Parallel Quad SPI
H24	PMC_MIO9_500	qspi1_io[1]	Dual-Parallel Quad SPI
G24	PMC_MIO10_500	qspi1_io[2]	Dual-Parallel Quad SPI
G23	PMC_MIO11_500	qspi1_io[3]	Dual-Parallel Quad SPI
H23	PMC_MIO12_500	qspi1_clk	Dual-Parallel Quad SPI
J23	PMC_MIO13_500	usb_ulpi_rst	USB 2.0
K23	PMC_MIO14_500	usb_ulpi_data[0]	USB 2.0
M23	PMC_MIO15_500	usb_ulpi_data[1]	USB 2.0
N23	PMC_MIO16_500	usb_ulpi_data[2]	USB 2.0
M22	PMC_MIO17_500	usb_ulpi_data[3]	USB 2.0
L22	PMC_MIO18_500	usb_ulpi_clk	USB 2.0
K22	PMC_MIO19_500	usb_ulpi_data[4]	USB 2.0
J22	PMC_MIO20_500	usb_ulpi_data[5]	USB 2.0
G22	PMC_MIO21_500	usb_ulpi_data[6]	USB 2.0
G21	PMC_MIO22_500	usb_ulpi_data[7]	USB 2.0
M21	PMC_MIO23_500	usb_ulpi_dir	USB 2.0
N21	PMC_MIO24_500	usb_ulpi_stp	USB 2.0
N20	PMC_MIO25_500	usb_ulpi_nxt	USB 2.0
E29	PMC_MIO26_501	sdio_1v8_clk	SD1_3.0
K29	PMC_MIO27_501	NC	-
L29	PMC_MIO28_501	sdio_1v8_detect	SD1_3.0
M29	PMC_MIO29_501	sdio_1v8_cmd	SD1_3.0
N29	PMC_MIO30_501	sdio_1v8_dat0	SD1_3.0
N28	PMC_MIO31_501	sdio_1v8_dat1	SD1_3.0
M28	PMC_MIO32_501	sdio_1v8_dat2	SD1_3.0
K28	PMC_MIO33_501	sdio_1v8_dat3	SD1_3.0

Table 11 : MIO Map (continued on next page)

Pin Number	Pin Name	Signal Name	Comment
J28	PMC_MIO34_501	sdio_1v8_sel	SD1_3.0
H28	PMC_MIO35_501	NC	-
G28	PMC_MIO36_501	NC	-
E28	PMC_MIO37_501	gem0_rst_mio_l	GEM0 Ethernet
E27	PMC_MIO38_501	PCIE_RST_1V8_L	PCIE
F27	PMC_MIO39_501	PCIE_RST_1V8_L	PCIE
G27	PMC_MIO40_501	NC	-
J27	PMC_MIO41_501	NC	-
K27	PMC_MIO42_501	uart0_rxd	Not available until full power
L27	PMC_MIO43_501	uart0_txd	Not available until full power
M27	PMC_MIO44_501	NC	-
N26	PMC_MIO45_501	NC	-
M26	PMC_MIO46_501	uart1_txd	Available with aux. power
L26	PMC_MIO47_501	uart1_rxd	Available with aux. power
J26	PMC_MIO48_501	NC	-
H26	PMC_MIO49_501	pmc_smon_scl	PMC System Monitor
G26	PMC_MIO50_501	pmc_smon_sda	PMC System Monitor
F26	PMC_MIO51_501	NC	-
D26	LPD_MIO0_502	gem0_tx_clk	GEM0 Ethernet
A25	LPD_MIO1_502	gem0_txd_0	GEM0 Ethernet
C25	LPD_MIO2_502	gem0_txd_1	GEM0 Ethernet
D25	LPD_MIO3_502	gem0_txd_2	GEM0 Ethernet
E25	LPD_MIO4_502	gem0_txd_3	GEM0 Ethernet
F25	LPD_MIO5_502	gem0_tx_ctrl	GEM0 Ethernet
F24	LPD_MIO6_502	gem0_rx_clk	GEM0 Ethernet
E24	LPD_MIO7_502	gem0_rxd_0	GEM0 Ethernet
C24	LPD_MIO8_502	gem0_rxd_1	GEM0 Ethernet
B24	LPD_MIO9_502	gem0_rxd_2	GEM0 Ethernet
A24	LPD_MIO10_502	gem0_rxd_3	GEM0 Ethernet
B23	LPD_MIO11_502	gem0_rx_ctrl	GEM0 Ethernet
C23	LPD_MIO12_502	qsfp0_int_l	QSFP mode control
D23	LPD_MIO13_502	qsfp0_modprs_l	QSFP mode control
E23	LPD_MIO14_502	qsfp1_int_l	QSFP mode control
F22	LPD_MIO15_502	qsfp1_modprs_l	QSFP mode control
E22	LPD_MIO16_502	qsfp2_int_l	QSFP mode control
D22	LPD_MIO17_502	qsfp2_modprs_l	QSFP mode control

Table 11 : MIO Map (continued on next page)

Pin Number	Pin Name	Signal Name	Comment
B22	LPD_MIO18_502	fan_fail_l	Fan status
A22	LPD_MIO19_502	usr_sw_1	User Switch 1
A21	LPD_MIO20_502	NC	-
B21	LPD_MIO21_502	NC	-
C21	LPD_MIO22_502	NC	-
D21	LPD_MIO23_502	NC	-
F21	LPD_MIO24_502	gem0_mdc	GEM0 Ethernet
E20	LPD_MIO25_502	gem0_mdio	GEM0 Ethernet

Table 11 : MIO Map

Appendix B: Complete Pinout Table

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
AR12	NC	GTYP_LPD_REFCLKN1_102	MGT	102
AR13	NC	GTYP_LPD_REFCLKP1_102	MGT	102
AU12	pcie_refclk_0_n	GTYP_LPD_REFCLKN0_102	MGT	102
AU13	pcie_refclk_0_p	GTYP_LPD_REFCLKP0_102	MGT	102
AL1	pcie_rx15_n	GTYP_LPD_RXN0_102	MGT	102
AL2	pcie_rx15_p	GTYP_LPD_RXP0_102	MGT	102
AJ1	pcie_rx14_n	GTYP_LPD_RXN1_102	MGT	102
AJ2	pcie_rx14_p	GTYP_LPD_RXP1_102	MGT	102
AH3	pcie_rx13_n	GTYP_LPD_RXN2_102	MGT	102
AH4	pcie_rx13_p	GTYP_LPD_RXP2_102	MGT	102
AG1	pcie_rx12_n	GTYP_LPD_RXN3_102	MGT	102
AG2	pcie_rx12_p	GTYP_LPD_RXP3_102	MGT	102
AN6	pcie_tx15_n	GTYP_LPD_TXN0_102	MGT	102
AN7	pcie_tx15_p	GTYP_LPD_TXP0_102	MGT	102
AM4	pcie_tx14_n	GTYP_LPD_TXN1_102	MGT	102
AM5	pcie_tx14_p	GTYP_LPD_TXP1_102	MGT	102
AM8	pcie_tx13_n	GTYP_LPD_TXN2_102	MGT	102
AM9	pcie_tx13_p	GTYP_LPD_TXP2_102	MGT	102
AL6	pcie_tx12_n	GTYP_LPD_TXN3_102	MGT	102
AL7	pcie_tx12_p	GTYP_LPD_TXP3_102	MGT	102
AL10	NC	GTYP_LPD_REFCLKN1_103	MGT	103
AL11	NC	GTYP_LPD_REFCLKP1_103	MGT	103
AN10	pcie_lcl_refclk_n	GTYP_LPD_REFCLKN0_103	MGT	103
AN11	pcie_lcl_refclk_p	GTYP_LPD_REFCLKP0_103	MGT	103
AF3	pcie_rx11_n	GTYP_LPD_RXN0_103	MGT	103
AF4	pcie_rx11_p	GTYP_LPD_RXP0_103	MGT	103
AE1	pcie_rx10_n	GTYP_LPD_RXN1_103	MGT	103
AE2	pcie_rx10_p	GTYP_LPD_RXP1_103	MGT	103
AD3	pcie_rx9_n	GTYP_LPD_RXN2_103	MGT	103
AD4	pcie_rx9_p	GTYP_LPD_RXP2_103	MGT	103
AC1	pcie_rx8_n	GTYP_LPD_RXN3_103	MGT	103
AC2	pcie_rx8_p	GTYP_LPD_RXP3_103	MGT	103
AK4	pcie_tx11_n	GTYP_LPD_TXN0_103	MGT	103

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
AK5	pcie_tx11_p	GTYP_LPD_TXP0_103	MGT	103
AJ6	pcie_tx10_n	GTYP_LPD_TXN1_103	MGT	103
AJ7	pcie_tx10_p	GTYP_LPD_TXP1_103	MGT	103
AH8	pcie_tx9_n	GTYP_LPD_TXN2_103	MGT	103
AH9	pcie_tx9_p	GTYP_LPD_TXP2_103	MGT	103
AG6	pcie_tx8_n	GTYP_LPD_TXN3_103	MGT	103
AG7	pcie_tx8_p	GTYP_LPD_TXP3_103	MGT	103
AJ10	NC	GTYP_LPD_REFCLKN1_104	MGT	104
AJ11	NC	GTYP_LPD_REFCLKP1_104	MGT	104
AK8	pcie_refclk_1_n	GTYP_LPD_REFCLKN0_104	MGT	104
AK9	pcie_refclk_1_p	GTYP_LPD_REFCLKP0_104	MGT	104
Y3	pcie_rx5_n	GTYP_LPD_RXN2_104	MGT	104
Y4	pcie_rx5_p	GTYP_LPD_RXP2_104	MGT	104
W1	pcie_rx4_n	GTYP_LPD_RXN3_104	MGT	104
W2	pcie_rx4_p	GTYP_LPD_RXP3_104	MGT	104
AB3	pcie_rx7_n	GTYP_LPD_RXN0_104	MGT	104
AB4	pcie_rx7_p	GTYP_LPD_RXP0_104	MGT	104
AA1	pcie_rx6_n	GTYP_LPD_RXN1_104	MGT	104
AA2	pcie_rx6_p	GTYP_LPD_RXP1_104	MGT	104
AC6	pcie_tx5_n	GTYP_LPD_TXN2_104	MGT	104
AC7	pcie_tx5_p	GTYP_LPD_TXP2_104	MGT	104
AA6	pcie_tx4_n	GTYP_LPD_TXN3_104	MGT	104
AA7	pcie_tx4_p	GTYP_LPD_TXP3_104	MGT	104
AF8	pcie_tx7_n	GTYP_LPD_TXN0_104	MGT	104
AF9	pcie_tx7_p	GTYP_LPD_TXP0_104	MGT	104
AE6	pcie_tx6_n	GTYP_LPD_TXN1_104	MGT	104
AE7	pcie_tx6_p	GTYP_LPD_TXP1_104	MGT	104
AE10	NC	GTYP_LPD_REFCLKN0_105	MGT	105
AD8	NC	GTYP_LPD_REFCLKN1_105	MGT	105
AE11	NC	GTYP_LPD_REFCLKP0_105	MGT	105
AD9	NC	GTYP_LPD_REFCLKP1_105	MGT	105
U1	pcie_rx3_n	GTYP_LPD_RXN0_105	MGT	105
U2	pcie_rx3_p	GTYP_LPD_RXP0_105	MGT	105
R1	pcie_rx2_n	GTYP_LPD_RXN1_105	MGT	105
R2	pcie_rx2_p	GTYP_LPD_RXP1_105	MGT	105
N1	pcie_rx1_n	GTYP_LPD_RXN2_105	MGT	105

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
N2	pcie_rx1_p	GTYP_LPD_RXP2_105	MGT	105
L1	pcie_rx0_n	GTYP_LPD_RXN3_105	MGT	105
L2	pcie_rx0_p	GTYP_LPD_RXP3_105	MGT	105
W6	pcie_tx3_n	GTYP_LPD_TXN0_105	MGT	105
W7	pcie_tx3_p	GTYP_LPD_TXP0_105	MGT	105
V4	pcie_tx2_n	GTYP_LPD_TXN1_105	MGT	105
V5	pcie_tx2_p	GTYP_LPD_TXP1_105	MGT	105
U6	pcie_tx1_n	GTYP_LPD_TXN2_105	MGT	105
U7	pcie_tx1_p	GTYP_LPD_TXP2_105	MGT	105
T4	pcie_tx0_n	GTYP_LPD_TXN3_105	MGT	105
T5	pcie_tx0_p	GTYP_LPD_TXP3_105	MGT	105
Y8	mgt_progclk_0_n	GTM_REFCLKN0_109	MGT	109
W10	si5402_out6_n	GTM_REFCLKN1_109	MGT	109
Y9	mgt_progclk_0_p	GTM_REFCLKP0_109	MGT	109
W11	si5402_out6_p	GTM_REFCLKP1_109	MGT	109
G5	qsfp2_tx0_n	GTM_TXN0_109	MGT	109
J6	qsfp2_tx1_n	GTM_TXN1_109	MGT	109
G7	qsfp2_tx2_n	GTM_TXN2_109	MGT	109
J8	qsfp2_tx3_n	GTM_TXN3_109	MGT	109
H5	qsfp2_tx0_p	GTM_TXP0_109	MGT	109
K6	qsfp2_tx1_p	GTM_TXP1_109	MGT	109
H7	qsfp2_tx2_p	GTM_TXP2_109	MGT	109
K8	qsfp2_tx3_p	GTM_TXP3_109	MGT	109
D4	qsfp2_rx0_n	GTM_RXN0_109	MGT	109
B5	qsfp2_rx1_n	GTM_RXN1_109	MGT	109
D6	qsfp2_rx2_n	GTM_RXN2_109	MGT	109
B7	qsfp2_rx3_n	GTM_RXN3_109	MGT	109
E4	qsfp2_rx0_p	GTM_RXP0_109	MGT	109
C5	qsfp2_rx1_p	GTM_RXP1_109	MGT	109
E6	qsfp2_rx2_p	GTM_RXP2_109	MGT	109
C7	qsfp2_rx3_p	GTM_RXP3_109	MGT	109
U10	si5344_out0_n	GTM_REFCLKN0_110	MGT	110
T8	si5402_out7_n	GTM_REFCLKN1_110	MGT	110
U11	si5344_out0_p	GTM_REFCLKP0_110	MGT	110
T9	si5402_out7_p	GTM_REFCLKP1_110	MGT	110
G9	qsfp2_tx4_n	GTM_TXN0_110	MGT	110

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
J10	qsfp2_tx5_n	GTM_TXN1_110	MGT	110
G11	qsfp2_tx6_n	GTM_TXN2_110	MGT	110
J12	qsfp2_tx7_n	GTM_TXN3_110	MGT	110
H9	qsfp2_tx4_p	GTM_TXP0_110	MGT	110
K10	qsfp2_tx5_p	GTM_TXP1_110	MGT	110
H11	qsfp2_tx6_p	GTM_TXP2_110	MGT	110
K12	qsfp2_tx7_p	GTM_TXP3_110	MGT	110
D8	qsfp2_rx4_n	GTM_RXN0_110	MGT	110
B9	qsfp2_rx5_n	GTM_RXN1_110	MGT	110
D10	qsfp2_rx6_n	GTM_RXN2_110	MGT	110
B11	qsfp2_rx7_n	GTM_RXN3_110	MGT	110
E8	qsfp2_rx4_p	GTM_RXP0_110	MGT	110
C9	qsfp2_rx5_p	GTM_RXP1_110	MGT	110
E10	qsfp2_rx6_p	GTM_RXP2_110	MGT	110
C11	qsfp2_rx7_p	GTM_RXP3_110	MGT	110
BA45	mgt_progclk_2_n	GTYP_REFCLKN0_200	MGT	200
BA44	mgt_progclk_2_p	GTYP_REFCLKP0_200	MGT	200
BC56	qsfp0_rx0_n	GTYP_RXN0_200	MGT	200
BC55	qsfp0_rx0_p	GTYP_RXP0_200	MGT	200
BB58	qsfp0_rx1_n	GTYP_RXN1_200	MGT	200
BB57	qsfp0_rx1_p	GTYP_RXP1_200	MGT	200
BA56	qsfp0_rx2_n	GTYP_RXN2_200	MGT	200
BA55	qsfp0_rx2_p	GTYP_RXP2_200	MGT	200
AY58	qsfp0_rx3_n	GTYP_RXN3_200	MGT	200
AY57	qsfp0_rx3_p	GTYP_RXP3_200	MGT	200
BC53	qsfp0_tx0_n	GTYP_TXN0_200	MGT	200
BC52	qsfp0_tx0_p	GTYP_TXP0_200	MGT	200
BC49	qsfp0_tx1_n	GTYP_TXN1_200	MGT	200
BC48	qsfp0_tx1_p	GTYP_TXP1_200	MGT	200
BB51	qsfp0_tx2_n	GTYP_TXN2_200	MGT	200
BB50	qsfp0_tx2_p	GTYP_TXP2_200	MGT	200
BA53	qsfp0_tx3_n	GTYP_TXN3_200	MGT	200
BA52	qsfp0_tx3_p	GTYP_TXP3_200	MGT	200
AY47	si5402_out1_n	GTYP_REFCLKN1_200	MGT	200
AY46	si5402_out1_p	GTYP_REFCLKP1_200	MGT	200
AW56	qsfp0_rx4_n	GTYP_RXN0_201	MGT	201

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
AW55	qsfp0_rx4_p	GTYP_RXP0_201	MGT	201
AV58	qsfp0_rx5_n	GTYP_RXN1_201	MGT	201
AV57	qsfp0_rx5_p	GTYP_RXP1_201	MGT	201
AU56	qsfp0_rx6_n	GTYP_RXN2_201	MGT	201
AU55	qsfp0_rx6_p	GTYP_RXP2_201	MGT	201
AT58	qsfp0_rx7_n	GTYP_RXN3_201	MGT	201
AT57	qsfp0_rx7_p	GTYP_RXP3_201	MGT	201
BA49	qsfp0_tx4_n	GTYP_TXN0_201	MGT	201
BA48	qsfp0_tx4_p	GTYP_TXP0_201	MGT	201
AY51	qsfp0_tx5_n	GTYP_TXN1_201	MGT	201
AY50	qsfp0_tx5_p	GTYP_TXP1_201	MGT	201
AW53	qsfp0_tx6_n	GTYP_TXN2_201	MGT	201
AW52	qsfp0_tx6_p	GTYP_TXP2_201	MGT	201
AW49	qsfp0_tx7_n	GTYP_TXN3_201	MGT	201
AW48	qsfp0_tx7_p	GTYP_TXP3_201	MGT	201
AV47	si5344_out2_n	GTYP_REFCLKN0_201	MGT	201
AV46	si5344_out2_p	GTYP_REFCLKP0_201	MGT	201
AT47	si5402_out2_n	GTYP_REFCLKN1_201	MGT	201
AT46	si5402_out2_p	GTYP_REFCLKP1_201	MGT	201
W49	si5344_out1_n	GTM_REFCLKN0_209	MGT	209
V51	si5402_out3_n	GTM_REFCLKN1_209	MGT	209
W48	si5344_out1_p	GTM_REFCLKP0_209	MGT	209
V50	si5402_out3_p	GTM_REFCLKP1_209	MGT	209
J45	qsfp1_tx0_n	GTM_TXN0_209	MGT	209
G44	qsfp1_tx1_n	GTM_TXN1_209	MGT	209
J43	qsfp1_tx2_n	GTM_TXN2_209	MGT	209
G42	qsfp1_tx3_n	GTM_TXN3_209	MGT	209
K45	qsfp1_tx0_p	GTM_TXP0_209	MGT	209
H44	qsfp1_tx1_p	GTM_TXP1_209	MGT	209
K43	qsfp1_tx2_p	GTM_TXP2_209	MGT	209
H42	qsfp1_tx3_p	GTM_TXP3_209	MGT	209
B46	qsfp1_rx0_n	GTM_RXN0_209	MGT	209
D45	qsfp1_rx1_n	GTM_RXN1_209	MGT	209
B44	qsfp1_rx2_n	GTM_RXN2_209	MGT	209
D43	qsfp1_rx3_n	GTM_RXN3_209	MGT	209
C46	qsfp1_rx0_p	GTM_RXP0_209	MGT	209

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
E45	qsfp1_rx1_p	GTM_RXP1_209	MGT	209
C44	qsfp1_rx2_p	GTM_RXP2_209	MGT	209
E43	qsfp1_rx3_p	GTM_RXP3_209	MGT	209
U49	mgt_progclk_1_n	GTM_REFCLKN0_210	MGT	210
T51	si5402_out4_n	GTM_REFCLKN1_210	MGT	210
U48	mgt_progclk_1_p	GTM_REFCLKP0_210	MGT	210
T50	si5402_out4_p	GTM_REFCLKP1_210	MGT	210
J41	qsfp1_tx4_n	GTM_TXN0_210	MGT	210
G40	qsfp1_tx5_n	GTM_TXN1_210	MGT	210
J39	qsfp1_tx6_n	GTM_TXN2_210	MGT	210
G38	qsfp1_tx7_n	GTM_TXN3_210	MGT	210
K41	qsfp1_tx4_p	GTM_TXP0_210	MGT	210
H40	qsfp1_tx5_p	GTM_TXP1_210	MGT	210
K39	qsfp1_tx6_p	GTM_TXP2_210	MGT	210
H38	qsfp1_tx7_p	GTM_TXP3_210	MGT	210
B42	qsfp1_rx4_n	GTM_RXN0_210	MGT	210
D41	qsfp1_rx5_n	GTM_RXN1_210	MGT	210
B40	qsfp1_rx6_n	GTM_RXN2_210	MGT	210
D39	qsfp1_rx7_n	GTM_RXN3_210	MGT	210
C42	qsfp1_rx4_p	GTM_RXP0_210	MGT	210
E41	qsfp1_rx5_p	GTM_RXP1_210	MGT	210
C40	qsfp1_rx6_p	GTM_RXP2_210	MGT	210
E39	qsfp1_rx7_p	GTM_RXP3_210	MGT	210
AY9	lpddr4_0_ch0_ca_a[0]	IO_L22N_N7P3_M0P45_700	1.1V	700
AY10	lpddr4_0_ch0_ca_a[1]	IO_L22P_N7P2_M0P44_700	1.1V	700
AV10	lpddr4_0_ch0_ca_a[2]	IO_L21P_XCC_N7P0_M0P42_700	1.1V	700
AT9	lpddr4_0_ch0_ca_a[3]	IO_L23N_N7P5_M0P47_700	1.1V	700
AW11	lpddr4_0_ch0_ca_a[4]	IO_L19P_N6P2_M0P38_700	1.1V	700
AW10	lpddr4_0_ch0_ca_a[5]	IO_L19N_N6P3_M0P39_700	1.1V	700
AT7	lpddr4_0_ch0_ca_b[0]	IO_L16P_N5P2_M0P32_700	1.1V	700
AW8	lpddr4_0_ch0_ca_b[1]	IO_L14N_N4P5_M0P29_700	1.1V	700
AW6	lpddr4_0_ch0_ca_b[2]	IO_L17N_N5P5_M0P35_700	1.1V	700
AW7	lpddr4_0_ch0_ca_b[3]	IO_L17P_N5P4_M0P34_700	1.1V	700
AY7	lpddr4_0_ch0_ca_b[4]	IO_L13N_N4P3_M0P27_700	1.1V	700
AY8	lpddr4_0_ch0_ca_b[5]	IO_L13P_N4P2_M0P26_700	1.1V	700
AY12	lpddr4_0_ch0_ck_c_a[0]	IO_L18N_XCC_N6P1_M0P37_700	1.1V	700

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
AU8	lpddr4_0_ch0_ck_c_b[0]	IO_L12N_GC_XCC_N4P1_M0P25_700	1.1V	700
AW12	lpddr4_0_ch0_ck_t_a[0]	IO_L18P_XCC_N6P0_M0P36_700	1.1V	700
AU9	lpddr4_0_ch0_ck_t_b[0]	IO_L12P_GC_XCC_N4P0_M0P24_700	1.1V	700
AR10	lpddr4_0_ch0_cke_a[0]	IO_L20P_N6P4_M0P40_700	1.1V	700
AT10	lpddr4_0_ch0_cke_a[1]	IO_L20N_N6P5_M0P41_700	1.1V	700
AV8	lpddr4_0_ch0_cke_b[0]	IO_L14P_N4P4_M0P28_700	1.1V	700
AU7	lpddr4_0_ch0_cke_b[1]	IO_L16N_N5P3_M0P33_700	1.1V	700
AR9	lpddr4_0_ch0_cs_a[0]	IO_L23P_N7P4_M0P46_700	1.1V	700
AV9	lpddr4_0_ch0_cs_a[1]	IO_L21N_XCC_N7P1_M0P43_700	1.1V	700
AW2	lpddr4_0_ch0_cs_b[0]	IO_L0N_XCC_N0P1_M0P1_700	1.1V	700
AR4	lpddr4_0_ch0_cs_b[1]	IO_L9N_GC_XCC_N3P1_M0P19_700	1.1V	700
AP4	lpddr4_0_ch0_dmi_a[0]	IO_L9P_GC_XCC_N3P0_M0P18_700	1.1V	700
AW3	lpddr4_0_ch0_dmi_b[0]	IO_L0P_XCC_N0P0_M0P0_700	1.1V	700
AV4	lpddr4_0_ch0_dq_a[0]	IO_L7N_N2P3_M0P15_700	1.1V	700
AW5	lpddr4_0_ch0_dq_a[7]	IO_L7P_N2P2_M0P14_700	1.1V	700
AU4	lpddr4_0_ch0_dq_a[2]	IO_L8N_N2P5_M0P17_700	1.1V	700
AT4	lpddr4_0_ch0_dq_a[3]	IO_L8P_N2P4_M0P16_700	1.1V	700
AR3	lpddr4_0_ch0_dq_a[4]	IO_L10N_N3P3_M0P21_700	1.1V	700
AV3	lpddr4_0_ch0_dq_a[1]	IO_L11N_N3P5_M0P23_700	1.1V	700
AP3	lpddr4_0_ch0_dq_a[5]	IO_L10P_N3P2_M0P20_700	1.1V	700
AU3	lpddr4_0_ch0_dq_a[6]	IO_L11P_N3P4_M0P22_700	1.1V	700
AP2	lpddr4_0_ch0_dq_b[0]	IO_L2P_N0P4_M0P4_700	1.1V	700
AR2	lpddr4_0_ch0_dq_b[1]	IO_L2N_N0P5_M0P5_700	1.1V	700
AT1	lpddr4_0_ch0_dq_b[2]	IO_L4P_N1P2_M0P8_700	1.1V	700
AU2	lpddr4_0_ch0_dq_b[3]	IO_L1N_N0P3_M0P3_700	1.1V	700
AU1	lpddr4_0_ch0_dq_b[4]	IO_L4N_N1P3_M0P9_700	1.1V	700
AV1	lpddr4_0_ch0_dq_b[5]	IO_L5P_N1P4_M0P10_700	1.1V	700
AW1	lpddr4_0_ch0_dq_b[6]	IO_L5N_N1P5_M0P11_700	1.1V	700
AT2	lpddr4_0_ch0_dq_b[7]	IO_L1P_N0P2_M0P2_700	1.1V	700
AT5	lpddr4_0_ch0_dqs_c_a[0]	IO_L6N_GC_XCC_N2P1_M0P13_700	1.1V	700
AP1	lpddr4_0_ch0_dqs_c_b[0]	IO_L3N_XCC_N1P1_M0P7_700	1.1V	700
AR5	lpddr4_0_ch0_dqs_t_a[0]	IO_L6P_GC_XCC_N2P0_M0P12_700	1.1V	700
AN1	lpddr4_0_ch0_dqs_t_b[0]	IO_L3P_XCC_N1P0_M0P6_700	1.1V	700
AV6	lpddr4_0_ch0_reset_n[0]	IO_L25P_N8P2_M0P50_700	1.1V	700
AV5	lpddr4_0_ch1_reset_n[0]	IO_L25N_N8P3_M0P51_700	1.1V	700
AU6	mem_clk_0_n	IO_L24N_GC_XCC_N8P1_M0P49_700	1.1V	700

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
AT6	mem_clk_0_p	IO_L24P_GC_XCC_N8P0_M0P48_700	1.1V	700
AR7	NC	IO_L15N_XCC_N5P1_M0P31_700	1.1V	700
AR8	NC	IO_L15P_XCC_N5P0_M0P30_700	1.1V	700
AY5	NC	IO_L26N_N8P5_M0P53_700	1.1V	700
AY6	NC	IO_L26P_N8P4_M0P52_700	1.1V	700
BA10	lpddr4_0_ch0_dmi_a[1]	IO_L15P_XCC_N5P0_M0P84_701	1.1V	701
BB3	lpddr4_0_ch0_dmi_b[1]	IO_L3P_XCC_N1P0_M0P60_701	1.1V	701
BC8	lpddr4_0_ch0_dq_a[15]	IO_L17N_N5P5_M0P89_701	1.1V	701
BC10	lpddr4_0_ch0_dq_a[13]	IO_L14N_N4P5_M0P83_701	1.1V	701
BA12	lpddr4_0_ch0_dq_a[9]	IO_L13P_N4P2_M0P80_701	1.1V	701
BB11	lpddr4_0_ch0_dq_a[10]	IO_L14P_N4P4_M0P82_701	1.1V	701
BB9	lpddr4_0_ch0_dq_a[8]	IO_L16P_N5P2_M0P86_701	1.1V	701
BA11	lpddr4_0_ch0_dq_a[11]	IO_L13N_N4P3_M0P81_701	1.1V	701
BB8	lpddr4_0_ch0_dq_a[12]	IO_L17P_N5P4_M0P88_701	1.1V	701
BC9	lpddr4_0_ch0_dq_a[14]	IO_L16N_N5P3_M0P87_701	1.1V	701
AY3	lpddr4_0_ch0_dq_b[14]	IO_L2N_N0P5_M0P59_701	1.1V	701
BA2	lpddr4_0_ch0_dq_b[8]	IO_L4N_N1P3_M0P63_701	1.1V	701
BA1	lpddr4_0_ch0_dq_b[12]	IO_L5P_N1P4_M0P64_701	1.1V	701
AY2	lpddr4_0_ch0_dq_b[13]	IO_L4P_N1P2_M0P62_701	1.1V	701
BC4	lpddr4_0_ch0_dq_b[9]	IO_L1N_N0P3_M0P57_701	1.1V	701
BB4	lpddr4_0_ch0_dq_b[11]	IO_L1P_N0P2_M0P56_701	1.1V	701
BB1	lpddr4_0_ch0_dq_b[10]	IO_L5N_N1P5_M0P65_701	1.1V	701
AY4	lpddr4_0_ch0_dq_b[15]	IO_L2P_N0P4_M0P58_701	1.1V	701
BB13	lpddr4_0_ch0_dqs_c_a[1]	IO_L12N_GC_XCC_N4P1_M0P79_701	1.1V	701
BA4	lpddr4_0_ch0_dqs_c_b[1]	IO_L0N_XCC_N0P1_M0P55_701	1.1V	701
BB14	lpddr4_0_ch0_dqs_t_a[1]	IO_L12P_GC_XCC_N4P0_M0P78_701	1.1V	701
BA5	lpddr4_0_ch0_dqs_t_b[1]	IO_L0P_XCC_N0P0_M0P54_701	1.1V	701
BC13	lpddr4_0_ch1_dmi_a[1]	IO_L18P_XCC_N6P0_M0P90_701	1.1V	701
BD3	lpddr4_0_ch1_dmi_b[1]	IO_L9P_GC_XCC_N3P0_M0P72_701	1.1V	701
BE13	lpddr4_0_ch1_dq_a[8]	IO_L19P_N6P2_M0P92_701	1.1V	701
BE11	lpddr4_0_ch1_dq_a[15]	IO_L20N_N6P5_M0P95_701	1.1V	701
BD7	lpddr4_0_ch1_dq_a[11]	IO_L23N_N7P5_M0P101_701	1.1V	701
BE8	lpddr4_0_ch1_dq_a[13]	IO_L22N_N7P3_M0P99_701	1.1V	701
BD12	lpddr4_0_ch1_dq_a[14]	IO_L19N_N6P3_M0P93_701	1.1V	701
BE9	lpddr4_0_ch1_dq_a[12]	IO_L22P_N7P2_M0P98_701	1.1V	701
BD11	lpddr4_0_ch1_dq_a[10]	IO_L20P_N6P4_M0P94_701	1.1V	701

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BD8	lpddr4_0_ch1_dq_a[9]	IO_L23P_N7P4_M0P100_701	1.1V	701
BB2	lpddr4_0_ch1_dq_b[10]	IO_L10P_N3P2_M0P74_701	1.1V	701
BC1	lpddr4_0_ch1_dq_b[8]	IO_L10N_N3P3_M0P75_701	1.1V	701
BD1	lpddr4_0_ch1_dq_b[9]	IO_L11N_N3P5_M0P77_701	1.1V	701
BE2	lpddr4_0_ch1_dq_b[13]	IO_L11P_N3P4_M0P76_701	1.1V	701
BE5	lpddr4_0_ch1_dq_b[14]	IO_L7N_N2P3_M0P69_701	1.1V	701
BD5	lpddr4_0_ch1_dq_b[15]	IO_L7P_N2P2_M0P68_701	1.1V	701
BE3	lpddr4_0_ch1_dq_b[11]	IO_L8N_N2P5_M0P71_701	1.1V	701
BE4	lpddr4_0_ch1_dq_b[12]	IO_L8P_N2P4_M0P70_701	1.1V	701
BE10	lpddr4_0_ch1_dqs_c_a[1]	IO_L21N_XCC_N7P1_M0P97_701	1.1V	701
BC5	lpddr4_0_ch1_dqs_c_b[1]	IO_L6N_GC_XCC_N2P1_M0P67_701	1.1V	701
BD10	lpddr4_0_ch1_dqs_t_a[1]	IO_L21P_XCC_N7P0_M0P96_701	1.1V	701
BC6	lpddr4_0_ch1_dqs_t_b[1]	IO_L6P_GC_XCC_N2P0_M0P66_701	1.1V	701
BA9	NC	IO_L15N_XCC_N5P1_M0P85_701	1.1V	701
BC12	NC	IO_L18N_XCC_N6P1_M0P91_701	1.1V	701
BB7	NC	IO_L24N_GC_XCC_N8P1_M0P103_701	1.1V	701
BA7	NC	IO_L24P_GC_XCC_N8P0_M0P102_701	1.1V	701
BD6	NC	IO_L25N_N8P3_M0P105_701	1.1V	701
BE7	NC	IO_L25P_N8P2_M0P104_701	1.1V	701
BB6	NC	IO_L26N_N8P5_M0P107_701	1.1V	701
BA6	NC	IO_L26P_N8P4_M0P106_701	1.1V	701
BC3	NC	IO_L3N_XCC_N1P1_M0P61_701	1.1V	701
BD2	NC	IO_L9N_GC_XCC_N3P1_M0P73_701	1.1V	701
BG1	lpddr4_0_ch1_ca_a[0]	IO_L4N_N1P3_M0P117_702	1.1V	702
BF1	lpddr4_0_ch1_ca_a[1]	IO_L4P_N1P2_M0P116_702	1.1V	702
BJ1	lpddr4_0_ch1_ca_a[2]	IO_L5N_N1P5_M0P119_702	1.1V	702
BH1	lpddr4_0_ch1_ca_a[3]	IO_L5P_N1P4_M0P118_702	1.1V	702
BL2	lpddr4_0_ch1_ca_a[4]	IO_L1P_N0P2_M0P110_702	1.1V	702
BL1	lpddr4_0_ch1_ca_a[5]	IO_L1N_N0P3_M0P111_702	1.1V	702
BG9	lpddr4_0_ch1_ca_b[0]	IO_L14P_N4P4_M0P136_702	1.1V	702
BH9	lpddr4_0_ch1_ca_b[1]	IO_L14N_N4P5_M0P137_702	1.1V	702
BG7	lpddr4_0_ch1_ca_b[2]	IO_L17N_N5P5_M0P143_702	1.1V	702
BK8	lpddr4_0_ch1_ca_b[3]	IO_L13N_N4P3_M0P135_702	1.1V	702
BK9	lpddr4_0_ch1_ca_b[4]	IO_L13P_N4P2_M0P134_702	1.1V	702
BF7	lpddr4_0_ch1_ca_b[5]	IO_L17P_N5P4_M0P142_702	1.1V	702
BK3	lpddr4_0_ch1_ck_c_a[0]	IO_L0N_XCC_N0P1_M0P109_702	1.1V	702

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BK10	lpddr4_0_ch1_ck_c_b[0]	IO_L12N_GC_XCC_N4P1_M0P133_702	1.1V	702
BJ3	lpddr4_0_ch1_ck_t_a[0]	IO_L0P_XCC_N0P0_M0P108_702	1.1V	702
BJ10	lpddr4_0_ch1_ck_t_b[0]	IO_L12P_GC_XCC_N4P0_M0P132_702	1.1V	702
BJ2	lpddr4_0_ch1_cke_a[0]	IO_L2P_N0P4_M0P112_702	1.1V	702
BG2	lpddr4_0_ch1_cke_a[1]	IO_L3N_XCC_N1P1_M0P115_702	1.1V	702
BH8	lpddr4_0_ch1_cke_b[0]	IO_L15N_XCC_N5P1_M0P139_702	1.1V	702
BG8	lpddr4_0_ch1_cke_b[1]	IO_L15P_XCC_N5P0_M0P138_702	1.1V	702
BF2	lpddr4_0_ch1_cs_a[0]	IO_L3P_XCC_N1P0_M0P114_702	1.1V	702
BK2	lpddr4_0_ch1_cs_a[1]	IO_L2N_N0P5_M0P113_702	1.1V	702
BF4	lpddr4_0_ch1_cs_b[0]	IO_L6N_GC_XCC_N2P1_M0P121_702	1.1V	702
BG11	lpddr4_0_ch1_cs_b[1]	IO_L21N_XCC_N7P1_M0P151_702	1.1V	702
BF5	lpddr4_0_ch1_dmi_a[0]	IO_L6P_GC_XCC_N2P0_M0P120_702	1.1V	702
BG12	lpddr4_0_ch1_dmi_b[0]	IO_L21P_XCC_N7P0_M0P150_702	1.1V	702
BG3	lpddr4_0_ch1_dq_a[3]	IO_L11P_N3P4_M0P130_702	1.1V	702
BH3	lpddr4_0_ch1_dq_a[2]	IO_L11N_N3P5_M0P131_702	1.1V	702
BJ5	lpddr4_0_ch1_dq_a[0]	IO_L7N_N2P3_M0P123_702	1.1V	702
BK5	lpddr4_0_ch1_dq_a[7]	IO_L8P_N2P4_M0P124_702	1.1V	702
BH4	lpddr4_0_ch1_dq_a[4]	IO_L10N_N3P3_M0P129_702	1.1V	702
BG4	lpddr4_0_ch1_dq_a[5]	IO_L10P_N3P2_M0P128_702	1.1V	702
BL5	lpddr4_0_ch1_dq_a[6]	IO_L8N_N2P5_M0P125_702	1.1V	702
BH5	lpddr4_0_ch1_dq_a[1]	IO_L7P_N2P2_M0P122_702	1.1V	702
BK12	lpddr4_0_ch1_dq_b[7]	IO_L20P_N6P4_M0P148_702	1.1V	702
BJ11	lpddr4_0_ch1_dq_b[4]	IO_L20N_N6P5_M0P149_702	1.1V	702
BH11	lpddr4_0_ch1_dq_b[2]	IO_L22P_N7P2_M0P152_702	1.1V	702
BJ13	lpddr4_0_ch1_dq_b[6]	IO_L19P_N6P2_M0P146_702	1.1V	702
BH10	lpddr4_0_ch1_dq_b[3]	IO_L22N_N7P3_M0P153_702	1.1V	702
BF9	lpddr4_0_ch1_dq_b[0]	IO_L23N_N7P5_M0P155_702	1.1V	702
BJ12	lpddr4_0_ch1_dq_b[5]	IO_L19N_N6P3_M0P147_702	1.1V	702
BF10	lpddr4_0_ch1_dq_b[1]	IO_L23P_N7P4_M0P154_702	1.1V	702
BL4	lpddr4_0_ch1_dqs_c_a[0]	IO_L9N_GC_XCC_N3P1_M0P127_702	1.1V	702
BF12	lpddr4_0_ch1_dqs_c_b[0]	IO_L18N_XCC_N6P1_M0P145_702	1.1V	702
BK4	lpddr4_0_ch1_dqs_t_a[0]	IO_L9P_GC_XCC_N3P0_M0P126_702	1.1V	702
BF13	lpddr4_0_ch1_dqs_t_b[0]	IO_L18P_XCC_N6P0_M0P144_702	1.1V	702
BT9	lpddr4_1_ch0_ca_a[0]	IO_L22N_N7P3_M1P45_703	1.1V	703
BT10	lpddr4_1_ch0_ca_a[1]	IO_L22P_N7P2_M1P44_703	1.1V	703
BP10	lpddr4_1_ch0_ca_a[2]	IO_L21P_XCC_N7P0_M1P42_703	1.1V	703

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BV9	lpddr4_1_ch0_ca_a[3]	IO_L23N_N7P5_M1P47_703	1.1V	703
BM11	lpddr4_1_ch0_ca_a[4]	IO_L19P_N6P2_M1P38_703	1.1V	703
BN10	lpddr4_1_ch0_ca_a[5]	IO_L19N_N6P3_M1P39_703	1.1V	703
BP8	lpddr4_1_ch0_ca_b[0]	IO_L16P_N5P2_M1P32_703	1.1V	703
BU8	lpddr4_1_ch0_ca_b[1]	IO_L14N_N4P5_M1P29_703	1.1V	703
BN8	lpddr4_1_ch0_ca_b[2]	IO_L17N_N5P5_M1P35_703	1.1V	703
BM8	lpddr4_1_ch0_ca_b[3]	IO_L17P_N5P4_M1P34_703	1.1V	703
BR8	lpddr4_1_ch0_ca_b[4]	IO_L13N_N4P3_M1P27_703	1.1V	703
BR9	lpddr4_1_ch0_ca_b[5]	IO_L13P_N4P2_M1P26_703	1.1V	703
BL11	lpddr4_1_ch0_ck_c_a[0]	IO_L18N_XCC_N6P1_M1P37_703	1.1V	703
BN9	lpddr4_1_ch0_ck_c_b[0]	IO_L12N_GC_XCC_N4P1_M1P25_703	1.1V	703
BL12	lpddr4_1_ch0_ck_t_a[0]	IO_L18P_XCC_N6P0_M1P36_703	1.1V	703
BM9	lpddr4_1_ch0_ck_t_b[0]	IO_L12P_GC_XCC_N4P0_M1P24_703	1.1V	703
BL10	lpddr4_1_ch0_cke_a[0]	IO_L20P_N6P4_M1P40_703	1.1V	703
BL9	lpddr4_1_ch0_cke_a[1]	IO_L20N_N6P5_M1P41_703	1.1V	703
BU9	lpddr4_1_ch0_cke_b[0]	IO_L14P_N4P4_M1P28_703	1.1V	703
BP7	lpddr4_1_ch0_cke_b[1]	IO_L16N_N5P3_M1P33_703	1.1V	703
BV10	lpddr4_1_ch0_cs_a[0]	IO_L23P_N7P4_M1P46_703	1.1V	703
BR10	lpddr4_1_ch0_cs_a[1]	IO_L21N_XCC_N7P1_M1P43_703	1.1V	703
BR3	lpddr4_1_ch0_cs_b[0]	IO_L0N_XCC_N0P1_M1P1_703	1.1V	703
BT5	lpddr4_1_ch0_cs_b[1]	IO_L9N_GC_XCC_N3P1_M1P19_703	1.1V	703
BR5	lpddr4_1_ch0_dmi_a[1]	IO_L9P_GC_XCC_N3P0_M1P18_703	1.1V	703
BR4	lpddr4_1_ch0_dmi_b[1]	IO_L0P_XCC_N0P0_M1P0_703	1.1V	703
BV6	lpddr4_1_ch0_dq_a[15]	IO_L8P_N2P4_M1P16_703	1.1V	703
BV5	lpddr4_1_ch0_dq_a[13]	IO_L8N_N2P5_M1P17_703	1.1V	703
BM4	lpddr4_1_ch0_dq_a[9]	IO_L11P_N3P4_M1P22_703	1.1V	703
BM3	lpddr4_1_ch0_dq_a[8]	IO_L11N_N3P5_M1P23_703	1.1V	703
BN5	lpddr4_1_ch0_dq_a[11]	IO_L10P_N3P2_M1P20_703	1.1V	703
BN4	lpddr4_1_ch0_dq_a[10]	IO_L10N_N3P3_M1P21_703	1.1V	703
BT6	lpddr4_1_ch0_dq_a[12]	IO_L7P_N2P2_M1P14_703	1.1V	703
BU6	lpddr4_1_ch0_dq_a[14]	IO_L7N_N2P3_M1P15_703	1.1V	703
BP1	lpddr4_1_ch0_dq_b[10]	IO_L5N_N1P5_M1P11_703	1.1V	703
BN1	lpddr4_1_ch0_dq_b[11]	IO_L5P_N1P4_M1P10_703	1.1V	703
BP3	lpddr4_1_ch0_dq_b[12]	IO_L2N_N0P5_M1P5_703	1.1V	703
BT4	lpddr4_1_ch0_dq_b[13]	IO_L1P_N0P2_M1P2_703	1.1V	703
BU4	lpddr4_1_ch0_dq_b[14]	IO_L1N_N0P3_M1P3_703	1.1V	703

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BN3	lpddr4_1_ch0_dq_b[15]	IO_L2P_N0P4_M1P4_703	1.1V	703
BR2	lpddr4_1_ch0_dq_b[8]	IO_L4N_N1P3_M1P9_703	1.1V	703
BP2	lpddr4_1_ch0_dq_b[9]	IO_L4P_N1P2_M1P8_703	1.1V	703
BP5	lpddr4_1_ch0_dqs_c_a[1]	IO_L6N_GC_XCC_N2P1_M1P13_703	1.1V	703
BM1	lpddr4_1_ch0_dqs_c_b[1]	IO_L3N_XCC_N1P1_M1P7_703	1.1V	703
BP6	lpddr4_1_ch0_dqs_t_a[1]	IO_L6P_GC_XCC_N2P0_M1P12_703	1.1V	703
BM2	lpddr4_1_ch0_dqs_t_b[1]	IO_L3P_XCC_N1P0_M1P6_703	1.1V	703
BR7	lpddr4_1_ch0_reset_n[0]	IO_L25P_N8P2_M1P50_703	1.1V	703
BT7	lpddr4_1_ch1_reset_n[0]	IO_L25N_N8P3_M1P51_703	1.1V	703
BM7	mem_clk_1_n	IO_L24N_GC_XCC_N8P1_M1P49_703	1.1V	703
BL7	mem_clk_1_p	IO_L24P_GC_XCC_N8P0_M1P48_703	1.1V	703
BK13	lpddr4_1_ch0_dmi_a[0]	IO_L15P_XCC_N5P0_M1P84_704	1.1V	704
BU12	lpddr4_1_ch0_dmi_b[0]	IO_L3P_XCC_N1P0_M1P60_704	1.1V	704
BG15	lpddr4_1_ch0_dq_a[0]	IO_L14P_N4P4_M1P82_704	1.1V	704
BH15	lpddr4_1_ch0_dq_a[1]	IO_L14N_N4P5_M1P83_704	1.1V	704
BF15	lpddr4_1_ch0_dq_a[2]	IO_L13N_N4P3_M1P81_704	1.1V	704
BE14	lpddr4_1_ch0_dq_a[3]	IO_L13P_N4P2_M1P80_704	1.1V	704
BM12	lpddr4_1_ch0_dq_a[4]	IO_L17P_N5P4_M1P88_704	1.1V	704
BM13	lpddr4_1_ch0_dq_a[5]	IO_L17N_N5P5_M1P89_704	1.1V	704
BM14	lpddr4_1_ch0_dq_a[6]	IO_L16N_N5P3_M1P87_704	1.1V	704
BL14	lpddr4_1_ch0_dq_a[7]	IO_L16P_N5P2_M1P86_704	1.1V	704
BU11	lpddr4_1_ch0_dq_b[0]	IO_L4P_N1P2_M1P62_704	1.1V	704
BV13	lpddr4_1_ch0_dq_b[1]	IO_L5P_N1P4_M1P64_704	1.1V	704
BV11	lpddr4_1_ch0_dq_b[2]	IO_L4N_N1P3_M1P63_704	1.1V	704
BV14	lpddr4_1_ch0_dq_b[3]	IO_L5N_N1P5_M1P65_704	1.1V	704
BR12	lpddr4_1_ch0_dq_b[4]	IO_L1P_N0P2_M1P56_704	1.1V	704
BT11	lpddr4_1_ch0_dq_b[5]	IO_L2P_N0P4_M1P58_704	1.1V	704
BT12	lpddr4_1_ch0_dq_b[6]	IO_L2N_N0P5_M1P59_704	1.1V	704
BR13	lpddr4_1_ch0_dq_b[7]	IO_L1N_N0P3_M1P57_704	1.1V	704
BD15	lpddr4_1_ch0_dqs_c_a[0]	IO_L12N_GC_XCC_N4P1_M1P79_704	1.1V	704
BP13	lpddr4_1_ch0_dqs_c_b[0]	IO_L0N_XCC_N0P1_M1P55_704	1.1V	704
BD14	lpddr4_1_ch0_dqs_t_a[0]	IO_L12P_GC_XCC_N4P0_M1P78_704	1.1V	704
BP12	lpddr4_1_ch0_dqs_t_b[0]	IO_L0P_XCC_N0P0_M1P54_704	1.1V	704
BD17	lpddr4_1_ch1_dmi_a[1]	IO_L18P_XCC_N6P0_M1P90_704	1.1V	704
BT15	lpddr4_1_ch1_dmi_b[1]	IO_L9P_GC_XCC_N3P0_M1P72_704	1.1V	704
BM17	lpddr4_1_ch1_dq_a[10]	IO_L23N_N7P5_M1P101_704	1.1V	704

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BL17	lpddr4_1_ch1_dq_a[11]	IO_L23P_N7P4_M1P100_704	1.1V	704
BG17	lpddr4_1_ch1_dq_a[12]	IO_L20P_N6P4_M1P94_704	1.1V	704
BH16	lpddr4_1_ch1_dq_a[13]	IO_L20N_N6P5_M1P95_704	1.1V	704
BF16	lpddr4_1_ch1_dq_a[14]	IO_L19N_N6P3_M1P93_704	1.1V	704
BE16	lpddr4_1_ch1_dq_a[15]	IO_L19P_N6P2_M1P92_704	1.1V	704
BJ15	lpddr4_1_ch1_dq_a[8]	IO_L22P_N7P2_M1P98_704	1.1V	704
BJ16	lpddr4_1_ch1_dq_a[9]	IO_L22N_N7P3_M1P99_704	1.1V	704
BV15	lpddr4_1_ch1_dq_b[10]	IO_L10N_N3P3_M1P75_704	1.1V	704
BR14	lpddr4_1_ch1_dq_b[11]	IO_L8P_N2P4_M1P70_704	1.1V	704
BR15	lpddr4_1_ch1_dq_b[12]	IO_L7N_N2P3_M1P69_704	1.1V	704
BP16	lpddr4_1_ch1_dq_b[13]	IO_L7P_N2P2_M1P68_704	1.1V	704
BV16	lpddr4_1_ch1_dq_b[14]	IO_L11N_N3P5_M1P77_704	1.1V	704
BU16	lpddr4_1_ch1_dq_b[15]	IO_L11P_N3P4_M1P76_704	1.1V	704
BT14	lpddr4_1_ch1_dq_b[8]	IO_L8N_N2P5_M1P71_704	1.1V	704
BU14	lpddr4_1_ch1_dq_b[9]	IO_L10P_N3P2_M1P74_704	1.1V	704
BK17	lpddr4_1_ch1_dqs_c_a[1]	IO_L21N_XCC_N7P1_M1P97_704	1.1V	704
BP15	lpddr4_1_ch1_dqs_c_b[1]	IO_L6N_GC_XCC_N2P1_M1P67_704	1.1V	704
BJ17	lpddr4_1_ch1_dqs_t_a[1]	IO_L21P_XCC_N7P0_M1P96_704	1.1V	704
BN15	lpddr4_1_ch1_dqs_t_b[1]	IO_L6P_GC_XCC_N2P0_M1P66_704	1.1V	704
BV19	lpddr4_1_ch1_ca_a[0]	IO_L4N_N1P3_M1P117_705	1.1V	705
BV18	lpddr4_1_ch1_ca_a[1]	IO_L4P_N1P2_M1P116_705	1.1V	705
BV21	lpddr4_1_ch1_ca_a[2]	IO_L5N_N1P5_M1P119_705	1.1V	705
BV20	lpddr4_1_ch1_ca_a[3]	IO_L5P_N1P4_M1P118_705	1.1V	705
BT19	lpddr4_1_ch1_ca_a[4]	IO_L1P_N0P2_M1P110_705	1.1V	705
BT20	lpddr4_1_ch1_ca_a[5]	IO_L1N_N0P3_M1P111_705	1.1V	705
BJ20	lpddr4_1_ch1_ca_b[0]	IO_L14P_N4P4_M1P136_705	1.1V	705
BJ21	lpddr4_1_ch1_ca_b[1]	IO_L14N_N4P5_M1P137_705	1.1V	705
BM22	lpddr4_1_ch1_ca_b[2]	IO_L17N_N5P5_M1P143_705	1.1V	705
BK22	lpddr4_1_ch1_ca_b[3]	IO_L13N_N4P3_M1P135_705	1.1V	705
BJ22	lpddr4_1_ch1_ca_b[4]	IO_L13P_N4P2_M1P134_705	1.1V	705
BL22	lpddr4_1_ch1_ca_b[5]	IO_L17P_N5P4_M1P142_705	1.1V	705
BU17	lpddr4_1_ch1_ck_c_a[0]	IO_L0N_XCC_N0P1_M1P109_705	1.1V	705
BH21	lpddr4_1_ch1_ck_c_b[0]	IO_L12N_GC_XCC_N4P1_M1P133_705	1.1V	705
BT17	lpddr4_1_ch1_ck_t_a[0]	IO_L0P_XCC_N0P0_M1P108_705	1.1V	705
BH20	lpddr4_1_ch1_ck_t_b[0]	IO_L12P_GC_XCC_N4P0_M1P132_705	1.1V	705
BT21	lpddr4_1_ch1_cke_a[0]	IO_L2P_N0P4_M1P112_705	1.1V	705

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BU19	lpddr4_1_ch1_cke_a[1]	IO_L3N_XCC_N1P1_M1P115_705	1.1V	705
BK18	lpddr4_1_ch1_cke_b[0]	IO_L15N_XCC_N5P1_M1P139_705	1.1V	705
BJ18	lpddr4_1_ch1_cke_b[1]	IO_L15P_XCC_N5P0_M1P138_705	1.1V	705
BU18	lpddr4_1_ch1_cs_a[0]	IO_L3P_XCC_N1P0_M1P114_705	1.1V	705
BU21	lpddr4_1_ch1_cs_a[1]	IO_L2N_N0P5_M1P113_705	1.1V	705
BP20	lpddr4_1_ch1_cs_b[0]	IO_L6N_GC_XCC_N2P1_M1P121_705	1.1V	705
BF21	lpddr4_1_ch1_cs_b[1]	IO_L21N_XCC_N7P1_M1P151_705	1.1V	705
BN20	lpddr4_1_ch1_dmi_a[0]	IO_L6P_GC_XCC_N2P0_M1P120_705	1.1V	705
BE20	lpddr4_1_ch1_dmi_b[0]	IO_L21P_XCC_N7P0_M1P150_705	1.1V	705
BR22	lpddr4_1_ch1_dq_a[0]	IO_L11P_N3P4_M1P130_705	1.1V	705
BT22	lpddr4_1_ch1_dq_a[1]	IO_L11N_N3P5_M1P131_705	1.1V	705
BR19	lpddr4_1_ch1_dq_a[5]	IO_L10P_N3P2_M1P128_705	1.1V	705
BP18	lpddr4_1_ch1_dq_a[6]	IO_L8N_N2P5_M1P125_705	1.1V	705
BP17	lpddr4_1_ch1_dq_a[4]	IO_L8P_N2P4_M1P124_705	1.1V	705
BR20	lpddr4_1_ch1_dq_a[2]	IO_L10N_N3P3_M1P129_705	1.1V	705
BP22	lpddr4_1_ch1_dq_a[7]	IO_L7N_N2P3_M1P123_705	1.1V	705
BP21	lpddr4_1_ch1_dq_a[3]	IO_L7P_N2P2_M1P122_705	1.1V	705
BD20	lpddr4_1_ch1_dq_b[0]	IO_L19P_N6P2_M1P146_705	1.1V	705
BD21	lpddr4_1_ch1_dq_b[1]	IO_L19N_N6P3_M1P147_705	1.1V	705
BF22	lpddr4_1_ch1_dq_b[2]	IO_L20N_N6P5_M1P149_705	1.1V	705
BE22	lpddr4_1_ch1_dq_b[3]	IO_L20P_N6P4_M1P148_705	1.1V	705
BF19	lpddr4_1_ch1_dq_b[4]	IO_L22N_N7P3_M1P153_705	1.1V	705
BF18	lpddr4_1_ch1_dq_b[5]	IO_L22P_N7P2_M1P152_705	1.1V	705
BG20	lpddr4_1_ch1_dq_b[6]	IO_L23P_N7P4_M1P154_705	1.1V	705
BG21	lpddr4_1_ch1_dq_b[7]	IO_L23N_N7P5_M1P155_705	1.1V	705
BR18	lpddr4_1_ch1_dqs_c_a[0]	IO_L9N_GC_XCC_N3P1_M1P127_705	1.1V	705
BE19	lpddr4_1_ch1_dqs_c_b[0]	IO_L18N_XCC_N6P1_M1P145_705	1.1V	705
BR17	lpddr4_1_ch1_dqs_t_a[0]	IO_L9P_GC_XCC_N3P0_M1P126_705	1.1V	705
BD18	lpddr4_1_ch1_dqs_t_b[0]	IO_L18P_XCC_N6P0_M1P144_705	1.1V	705
BM18	user_led_g0_1v1	IO_L24P_GC_XCC_N8P0_M1P156_705	1.1V	705
BM19	user_led_g1_1v1	IO_L24N_GC_XCC_N8P1_M1P157_705	1.1V	705
BN19	user_led_g2_1v1	IO_L26N_N8P5_M1P161_705	1.1V	705
BN21	user_led_g3_1v1	IO_L25N_N8P3_M1P159_705	1.1V	705
BN18	user_led_g4_1v1	IO_L26P_N8P4_M1P160_705	1.1V	705
BM21	user_led_g5_1v1	IO_L25P_N8P2_M1P158_705	1.1V	705
BG26	lpddr4_2_ch0_ca_a[0]	IO_L22N_N7P3_M2P45_706	1.1V	706

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BF25	lpddr4_2_ch0_ca_a[1]	IO_L22P_N7P2_M2P44_706	1.1V	706
BE23	lpddr4_2_ch0_ca_a[2]	IO_L21P_XCC_N7P0_M2P42_706	1.1V	706
BG27	lpddr4_2_ch0_ca_a[3]	IO_L23N_N7P5_M2P47_706	1.1V	706
BD26	lpddr4_2_ch0_ca_a[4]	IO_L19P_N6P2_M2P38_706	1.1V	706
BD27	lpddr4_2_ch0_ca_a[5]	IO_L19N_N6P3_M2P39_706	1.1V	706
BJ27	lpddr4_2_ch0_ca_b[0]	IO_L16P_N5P2_M2P32_706	1.1V	706
BK23	lpddr4_2_ch0_ca_b[1]	IO_L14N_N4P5_M2P29_706	1.1V	706
BM24	lpddr4_2_ch0_ca_b[2]	IO_L17N_N5P5_M2P35_706	1.1V	706
BL24	lpddr4_2_ch0_ca_b[3]	IO_L17P_N5P4_M2P34_706	1.1V	706
BJ26	lpddr4_2_ch0_ca_b[4]	IO_L13N_N4P3_M2P27_706	1.1V	706
BH26	lpddr4_2_ch0_ca_b[5]	IO_L13P_N4P2_M2P26_706	1.1V	706
BD24	lpddr4_2_ch0_ck_c_a[0]	IO_L18N_XCC_N6P1_M2P37_706	1.1V	706
BH25	lpddr4_2_ch0_ck_c_b[0]	IO_L12N_GC_XCC_N4P1_M2P25_706	1.1V	706
BD23	lpddr4_2_ch0_ck_t_a[0]	IO_L18P_XCC_N6P0_M2P36_706	1.1V	706
BG24	lpddr4_2_ch0_ck_t_b[0]	IO_L12P_GC_XCC_N4P0_M2P24_706	1.1V	706
BE25	lpddr4_2_ch0_cke_a[0]	IO_L20P_N6P4_M2P40_706	1.1V	706
BE26	lpddr4_2_ch0_cke_a[1]	IO_L20N_N6P5_M2P41_706	1.1V	706
BJ23	lpddr4_2_ch0_cke_b[0]	IO_L14P_N4P4_M2P28_706	1.1V	706
BK27	lpddr4_2_ch0_cke_b[1]	IO_L16N_N5P3_M2P33_706	1.1V	706
BF27	lpddr4_2_ch0_cs_a[0]	IO_L23P_N7P4_M2P46_706	1.1V	706
BF24	lpddr4_2_ch0_cs_a[1]	IO_L21N_XCC_N7P1_M2P43_706	1.1V	706
BT27	lpddr4_2_ch0_cs_b[0]	IO_L0N_XCC_N0P1_M2P1_706	1.1V	706
BR23	lpddr4_2_ch0_cs_b[1]	IO_L9N_GC_XCC_N3P1_M2P19_706	1.1V	706
BP23	lpddr4_2_ch0_dmi_a[1]	IO_L9P_GC_XCC_N3P0_M2P18_706	1.1V	706
BT26	lpddr4_2_ch0_dmi_b[1]	IO_L0P_XCC_N0P0_M2P0_706	1.1V	706
BT24	lpddr4_2_ch0_dq_a[9]	IO_L11P_N3P4_M2P22_706	1.1V	706
BT25	lpddr4_2_ch0_dq_a[11]	IO_L11N_N3P5_M2P23_706	1.1V	706
BR27	lpddr4_2_ch0_dq_a[12]	IO_L7N_N2P3_M2P15_706	1.1V	706
BP27	lpddr4_2_ch0_dq_a[13]	IO_L7P_N2P2_M2P14_706	1.1V	706
BP26	lpddr4_2_ch0_dq_a[14]	IO_L8N_N2P5_M2P17_706	1.1V	706
BR24	lpddr4_2_ch0_dq_a[15]	IO_L10P_N3P2_M2P20_706	1.1V	706
BP25	lpddr4_2_ch0_dq_a[8]	IO_L8P_N2P4_M2P16_706	1.1V	706
BR25	lpddr4_2_ch0_dq_a[10]	IO_L10N_N3P3_M2P21_706	1.1V	706
BU22	lpddr4_2_ch0_dq_b[10]	IO_L4P_N1P2_M2P8_706	1.1V	706
BU23	lpddr4_2_ch0_dq_b[11]	IO_L4N_N1P3_M2P9_706	1.1V	706
BV23	lpddr4_2_ch0_dq_b[9]	IO_L5P_N1P4_M2P10_706	1.1V	706

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BV24	lpddr4_2_ch0_dq_b[8]	IO_L5N_N1P5_M2P11_706	1.1V	706
BV28	lpddr4_2_ch0_dq_b[14]	IO_L1N_N0P3_M2P3_706	1.1V	706
BU26	lpddr4_2_ch0_dq_b[15]	IO_L2P_N0P4_M2P4_706	1.1V	706
BV26	lpddr4_2_ch0_dq_b[12]	IO_L2N_N0P5_M2P5_706	1.1V	706
BU27	lpddr4_2_ch0_dq_b[13]	IO_L1P_N0P2_M2P2_706	1.1V	706
BN25	lpddr4_2_ch0_dqs_c_a[1]	IO_L6N_GC_XCC_N2P1_M2P13_706	1.1V	706
BV25	lpddr4_2_ch0_dqs_c_b[1]	IO_L3N_XCC_N1P1_M2P7_706	1.1V	706
BN24	lpddr4_2_ch0_dqs_t_a[1]	IO_L6P_GC_XCC_N2P0_M2P12_706	1.1V	706
BU24	lpddr4_2_ch0_dqs_t_b[1]	IO_L3P_XCC_N1P0_M2P6_706	1.1V	706
BM26	lpddr4_2_ch0_reset_n[0]	IO_L25P_N8P2_M2P50_706	1.1V	706
BN26	lpddr4_2_ch1_reset_n[0]	IO_L25N_N8P3_M2P51_706	1.1V	706
BM27	mem_clk_2_n	IO_L24N_GC_XCC_N8P1_M2P49_706	1.1V	706
BL27	mem_clk_2_p	IO_L24P_GC_XCC_N8P0_M2P48_706	1.1V	706
BK24	NC	IO_L15N_XCC_N5P1_M2P31_706	1.1V	706
BJ25	NC	IO_L15P_XCC_N5P0_M2P30_706	1.1V	706
BN23	NC	IO_L26N_N8P5_M2P53_706	1.1V	706
BM23	NC	IO_L26P_N8P4_M2P52_706	1.1V	706
BH30	lpddr4_2_ch0_dmi_a[0]	IO_L15P_XCC_N5P0_M2P84_707	1.1V	707
BT29	lpddr4_2_ch0_dmi_b[0]	IO_L3P_XCC_N1P0_M2P60_707	1.1V	707
BF28	lpddr4_2_ch0_dq_a[6]	IO_L14N_N4P5_M2P83_707	1.1V	707
BK28	lpddr4_2_ch0_dq_a[4]	IO_L16N_N5P3_M2P87_707	1.1V	707
BJ28	lpddr4_2_ch0_dq_a[5]	IO_L16P_N5P2_M2P86_707	1.1V	707
BL29	lpddr4_2_ch0_dq_a[2]	IO_L17N_N5P5_M2P89_707	1.1V	707
BK29	lpddr4_2_ch0_dq_a[3]	IO_L17P_N5P4_M2P88_707	1.1V	707
BF30	lpddr4_2_ch0_dq_a[1]	IO_L13N_N4P3_M2P81_707	1.1V	707
BE29	lpddr4_2_ch0_dq_a[0]	IO_L13P_N4P2_M2P80_707	1.1V	707
BE28	lpddr4_2_ch0_dq_a[7]	IO_L14P_N4P4_M2P82_707	1.1V	707
BV29	lpddr4_2_ch0_dq_b[4]	IO_L5P_N1P4_M2P64_707	1.1V	707
BU29	lpddr4_2_ch0_dq_b[7]	IO_L4N_N1P3_M2P63_707	1.1V	707
BV30	lpddr4_2_ch0_dq_b[6]	IO_L5N_N1P5_M2P65_707	1.1V	707
BR30	lpddr4_2_ch0_dq_b[3]	IO_L2N_N0P5_M2P59_707	1.1V	707
BR29	lpddr4_2_ch0_dq_b[0]	IO_L2P_N0P4_M2P58_707	1.1V	707
BR28	lpddr4_2_ch0_dq_b[1]	IO_L1N_N0P3_M2P57_707	1.1V	707
BP28	lpddr4_2_ch0_dq_b[2]	IO_L1P_N0P2_M2P56_707	1.1V	707
BU28	lpddr4_2_ch0_dq_b[5]	IO_L4P_N1P2_M2P62_707	1.1V	707
BD30	lpddr4_2_ch0_dqs_c_a[0]	IO_L12N_GC_XCC_N4P1_M2P79_707	1.1V	707

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BN29	lpddr4_2_ch0_dqs_c_b[0]	IO_L0N_XCC_N0P1_M2P55_707	1.1V	707
BD29	lpddr4_2_ch0_dqs_t_a[0]	IO_L12P_GC_XCC_N4P0_M2P78_707	1.1V	707
BN28	lpddr4_2_ch0_dqs_t_b[0]	IO_L0P_XCC_N0P0_M2P54_707	1.1V	707
BD32	lpddr4_2_ch1_dmi_a[1]	IO_L18P_XCC_N6P0_M2P90_707	1.1V	707
BR32	lpddr4_2_ch1_dmi_b[1]	IO_L9P_GC_XCC_N3P0_M2P72_707	1.1V	707
BF31	lpddr4_2_ch1_dq_a[12]	IO_L20P_N6P4_M2P94_707	1.1V	707
BG30	lpddr4_2_ch1_dq_a[10]	IO_L20N_N6P5_M2P95_707	1.1V	707
BJ30	lpddr4_2_ch1_dq_a[8]	IO_L23P_N7P4_M2P100_707	1.1V	707
BE31	lpddr4_2_ch1_dq_a[13]	IO_L19P_N6P2_M2P92_707	1.1V	707
BJ31	lpddr4_2_ch1_dq_a[14]	IO_L23N_N7P5_M2P101_707	1.1V	707
BE32	lpddr4_2_ch1_dq_a[15]	IO_L19N_N6P3_M2P93_707	1.1V	707
BJ33	lpddr4_2_ch1_dq_a[11]	IO_L22N_N7P3_M2P99_707	1.1V	707
BJ32	lpddr4_2_ch1_dq_a[9]	IO_L22P_N7P2_M2P98_707	1.1V	707
BP30	lpddr4_2_ch1_dq_b[10]	IO_L7N_N2P3_M2P69_707	1.1V	707
BV31	lpddr4_2_ch1_dq_b[9]	IO_L11N_N3P5_M2P77_707	1.1V	707
BU32	lpddr4_2_ch1_dq_b[8]	IO_L11P_N3P4_M2P76_707	1.1V	707
BU31	lpddr4_2_ch1_dq_b[12]	IO_L10N_N3P3_M2P75_707	1.1V	707
BT31	lpddr4_2_ch1_dq_b[14]	IO_L10P_N3P2_M2P74_707	1.1V	707
BP31	lpddr4_2_ch1_dq_b[15]	IO_L8P_N2P4_M2P70_707	1.1V	707
BN30	lpddr4_2_ch1_dq_b[11]	IO_L7P_N2P2_M2P68_707	1.1V	707
BP32	lpddr4_2_ch1_dq_b[13]	IO_L8N_N2P5_M2P71_707	1.1V	707
BG32	lpddr4_2_ch1_dqs_c_a[1]	IO_L21N_XCC_N7P1_M2P97_707	1.1V	707
BN31	lpddr4_2_ch1_dqs_c_b[1]	IO_L6N_GC_XCC_N2P1_M2P67_707	1.1V	707
BF33	lpddr4_2_ch1_dqs_t_a[1]	IO_L21P_XCC_N7P0_M2P96_707	1.1V	707
BM31	lpddr4_2_ch1_dqs_t_b[1]	IO_L6P_GC_XCC_N2P0_M2P66_707	1.1V	707
BH31	NC	IO_L15N_XCC_N5P1_M2P85_707	1.1V	707
BD33	NC	IO_L18N_XCC_N6P1_M2P91_707	1.1V	707
BK33	NC	IO_L24N_GC_XCC_N8P1_M2P103_707	1.1V	707
BK32	NC	IO_L24P_GC_XCC_N8P0_M2P102_707	1.1V	707
BM32	NC	IO_L25N_N8P3_M2P105_707	1.1V	707
BL32	NC	IO_L25P_N8P2_M2P104_707	1.1V	707
BM28	NC	IO_L26P_N8P4_M2P106_707	1.1V	707
BT30	NC	IO_L3N_XCC_N1P1_M2P61_707	1.1V	707
BT32	NC	IO_L9N_GC_XCC_N3P1_M2P73_707	1.1V	707
BM29	spare_wp_1v1	IO_L26N_N8P5_M2P107_707	1.1V	707
BV34	lpddr4_2_ch1_ca_a[0]	IO_L4N_N1P3_M2P117_708	1.1V	708

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BV33	lpddr4_2_ch1_ca_a[1]	IO_L4P_N1P2_M2P116_708	1.1V	708
BV36	lpddr4_2_ch1_ca_a[2]	IO_L5N_N1P5_M2P119_708	1.1V	708
BV35	lpddr4_2_ch1_ca_a[3]	IO_L5P_N1P4_M2P118_708	1.1V	708
BT36	lpddr4_2_ch1_ca_a[4]	IO_L1P_N0P2_M2P110_708	1.1V	708
BT37	lpddr4_2_ch1_ca_a[5]	IO_L1N_N0P3_M2P111_708	1.1V	708
BJ35	lpddr4_2_ch1_ca_b[0]	IO_L14P_N4P4_M2P136_708	1.1V	708
BJ36	lpddr4_2_ch1_ca_b[1]	IO_L14N_N4P5_M2P137_708	1.1V	708
BM37	lpddr4_2_ch1_ca_b[2]	IO_L17N_N5P5_M2P143_708	1.1V	708
BJ38	lpddr4_2_ch1_ca_b[3]	IO_L13N_N4P3_M2P135_708	1.1V	708
BJ37	lpddr4_2_ch1_ca_b[4]	IO_L13P_N4P2_M2P134_708	1.1V	708
BL37	lpddr4_2_ch1_ca_b[5]	IO_L17P_N5P4_M2P142_708	1.1V	708
BT35	lpddr4_2_ch1_ck_c_a[0]	IO_L0N_XCC_N0P1_M2P109_708	1.1V	708
BH36	lpddr4_2_ch1_ck_c_b[0]	IO_L12N_GC_XCC_N4P1_M2P133_708	1.1V	708
BT34	lpddr4_2_ch1_ck_t_a[0]	IO_L0P_XCC_N0P0_M2P108_708	1.1V	708
BH35	lpddr4_2_ch1_ck_t_b[0]	IO_L12P_GC_XCC_N4P0_M2P132_708	1.1V	708
BU36	lpddr4_2_ch1_cke_a[0]	IO_L2P_N0P4_M2P112_708	1.1V	708
BU34	lpddr4_2_ch1_cke_a[1]	IO_L3N_XCC_N1P1_M2P115_708	1.1V	708
BL34	lpddr4_2_ch1_cke_b[0]	IO_L15N_XCC_N5P1_M2P139_708	1.1V	708
BK34	lpddr4_2_ch1_cke_b[1]	IO_L15P_XCC_N5P0_M2P138_708	1.1V	708
BU33	lpddr4_2_ch1_cs_a[0]	IO_L3P_XCC_N1P0_M2P114_708	1.1V	708
BU37	lpddr4_2_ch1_cs_a[1]	IO_L2N_N0P5_M2P113_708	1.1V	708
BN34	lpddr4_2_ch1_cs_b[0]	IO_L6N_GC_XCC_N2P1_M2P121_708	1.1V	708
BE35	lpddr4_2_ch1_cs_b[1]	IO_L21N_XCC_N7P1_M2P151_708	1.1V	708
BN33	lpddr4_2_ch1_dmi_a[0]	IO_L6P_GC_XCC_N2P0_M2P120_708	1.1V	708
BE34	lpddr4_2_ch1_dmi_b[0]	IO_L21P_XCC_N7P0_M2P150_708	1.1V	708
BR35	lpddr4_2_ch1_dq_a[5]	IO_L11N_N3P5_M2P131_708	1.1V	708
BR34	lpddr4_2_ch1_dq_a[6]	IO_L11P_N3P4_M2P130_708	1.1V	708
BP35	lpddr4_2_ch1_dq_a[2]	IO_L7N_N2P3_M2P123_708	1.1V	708
BN35	lpddr4_2_ch1_dq_a[1]	IO_L7P_N2P2_M2P122_708	1.1V	708
BR37	lpddr4_2_ch1_dq_a[4]	IO_L8N_N2P5_M2P125_708	1.1V	708
BP38	lpddr4_2_ch1_dq_a[3]	IO_L8P_N2P4_M2P124_708	1.1V	708
BP33	lpddr4_2_ch1_dq_a[0]	IO_L10P_N3P2_M2P128_708	1.1V	708
BR33	lpddr4_2_ch1_dq_a[7]	IO_L10N_N3P3_M2P129_708	1.1V	708
BD38	lpddr4_2_ch1_dq_b[0]	IO_L19P_N6P2_M2P146_708	1.1V	708
BF34	lpddr4_2_ch1_dq_b[3]	IO_L22P_N7P2_M2P152_708	1.1V	708
BE38	lpddr4_2_ch1_dq_b[2]	IO_L19N_N6P3_M2P147_708	1.1V	708

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BF36	lpddr4_2_ch1_dq_b[6]	IO_L23P_N7P4_M2P154_708	1.1V	708
BG36	lpddr4_2_ch1_dq_b[4]	IO_L23N_N7P5_M2P155_708	1.1V	708
BG35	lpddr4_2_ch1_dq_b[5]	IO_L22N_N7P3_M2P153_708	1.1V	708
BF37	lpddr4_2_ch1_dq_b[7]	IO_L20N_N6P5_M2P149_708	1.1V	708
BE37	lpddr4_2_ch1_dq_b[1]	IO_L20P_N6P4_M2P148_708	1.1V	708
BP37	lpddr4_2_ch1_dqs_c_a[0]	IO_L9N_GC_XCC_N3P1_M2P127_708	1.1V	708
BD36	lpddr4_2_ch1_dqs_c_b[0]	IO_L18N_XCC_N6P1_M2P145_708	1.1V	708
BP36	lpddr4_2_ch1_dqs_t_a[0]	IO_L9P_GC_XCC_N3P0_M2P126_708	1.1V	708
BD35	lpddr4_2_ch1_dqs_t_b[0]	IO_L18P_XCC_N6P0_M2P144_708	1.1V	708
BK38	NC	IO_L16N_N5P3_M2P141_708	1.1V	708
BK37	NC	IO_L16P_N5P2_M2P140_708	1.1V	708
BM34	NC	IO_L24N_GC_XCC_N8P1_M2P157_708	1.1V	708
BM33	NC	IO_L24P_GC_XCC_N8P0_M2P156_708	1.1V	708
BM36	NC	IO_L25P_N8P2_M2P158_708	1.1V	708
BN38	NC	IO_L26N_N8P5_M2P161_708	1.1V	708
BM38	qsfp2_lpmode_1v1	IO_L26P_N8P4_M2P160_708	1.1V	708
BN36	qsfp2_reset_1v1_l	IO_L25N_N8P3_M2P159_708	1.1V	708
BE41	lpddr4_3_ch1_ca_a[0]	IO_L19N_N6P3_M3P39_709	1.1V	709
BD41	lpddr4_3_ch1_ca_a[1]	IO_L19P_N6P2_M3P38_709	1.1V	709
BE40	lpddr4_3_ch1_ca_a[2]	IO_L20N_N6P5_M3P41_709	1.1V	709
BD39	lpddr4_3_ch1_ca_a[3]	IO_L20P_N6P4_M3P40_709	1.1V	709
BF42	lpddr4_3_ch1_ca_a[4]	IO_L22P_N7P2_M3P44_709	1.1V	709
BG42	lpddr4_3_ch1_ca_a[5]	IO_L22N_N7P3_M3P45_709	1.1V	709
BR38	lpddr4_3_ch1_ca_b[0]	IO_L11P_N3P4_M3P22_709	1.1V	709
BR39	lpddr4_3_ch1_ca_b[1]	IO_L11N_N3P5_M3P23_709	1.1V	709
BP42	lpddr4_3_ch1_ca_b[2]	IO_L8N_N2P5_M3P17_709	1.1V	709
BT40	lpddr4_3_ch1_ca_b[3]	IO_L10N_N3P3_M3P21_709	1.1V	709
BR40	lpddr4_3_ch1_ca_b[4]	IO_L10P_N3P2_M3P20_709	1.1V	709
BP41	lpddr4_3_ch1_ca_b[5]	IO_L8P_N2P4_M3P16_709	1.1V	709
BF43	lpddr4_3_ch1_ck_c_a[0]	IO_L21N_XCC_N7P1_M3P43_709	1.1V	709
BR43	lpddr4_3_ch1_ck_c_b[0]	IO_L9N_GC_XCC_N3P1_M3P19_709	1.1V	709
BE43	lpddr4_3_ch1_ck_t_a[0]	IO_L21P_XCC_N7P0_M3P42_709	1.1V	709
BP43	lpddr4_3_ch1_ck_t_b[0]	IO_L9P_GC_XCC_N3P0_M3P18_709	1.1V	709
BF39	lpddr4_3_ch1_cke_a[0]	IO_L23P_N7P4_M3P46_709	1.1V	709
BD42	lpddr4_3_ch1_cke_a[1]	IO_L18N_XCC_N6P1_M3P37_709	1.1V	709
BN43	lpddr4_3_ch1_cke_b[0]	IO_L6N_GC_XCC_N2P1_M3P13_709	1.1V	709

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BM43	lpddr4_3_ch1_cke_b[1]	IO_L6P_GC_XCC_N2P0_M3P12_709	1.1V	709
BC43	lpddr4_3_ch1_cs_a[0]	IO_L18P_XCC_N6P0_M3P36_709	1.1V	709
BF40	lpddr4_3_ch1_cs_a[1]	IO_L23N_N7P5_M3P47_709	1.1V	709
BJ41	lpddr4_3_ch1_cs_b[0]	IO_L15N_XCC_N5P1_M3P31_709	1.1V	709
BT42	lpddr4_3_ch1_cs_b[1]	IO_L0N_XCC_N0P1_M3P1_709	1.1V	709
BJ40	lpddr4_3_ch1_dmi_a[0]	IO_L15P_XCC_N5P0_M3P30_709	1.1V	709
BR42	lpddr4_3_ch1_dmi_b[0]	IO_L0P_XCC_N0P0_M3P0_709	1.1V	709
BG41	lpddr4_3_ch1_dq_a[1]	IO_L13P_N4P2_M3P26_709	1.1V	709
BK42	lpddr4_3_ch1_dq_a[6]	IO_L17P_N5P4_M3P34_709	1.1V	709
BK43	lpddr4_3_ch1_dq_a[7]	IO_L17N_N5P5_M3P35_709	1.1V	709
BJ42	lpddr4_3_ch1_dq_a[4]	IO_L14P_N4P4_M3P28_709	1.1V	709
BJ43	lpddr4_3_ch1_dq_a[5]	IO_L14N_N4P5_M3P29_709	1.1V	709
BL39	lpddr4_3_ch1_dq_a[2]	IO_L16N_N5P3_M3P33_709	1.1V	709
BK39	lpddr4_3_ch1_dq_a[3]	IO_L16P_N5P2_M3P32_709	1.1V	709
BH41	lpddr4_3_ch1_dq_a[0]	IO_L13N_N4P3_M3P27_709	1.1V	709
BV41	lpddr4_3_ch1_dq_b[3]	IO_L4N_N1P3_M3P9_709	1.1V	709
BT41	lpddr4_3_ch1_dq_b[4]	IO_L1P_N0P2_M3P2_709	1.1V	709
BU39	lpddr4_3_ch1_dq_b[1]	IO_L2N_N0P5_M3P5_709	1.1V	709
BT39	lpddr4_3_ch1_dq_b[6]	IO_L2P_N0P4_M3P4_709	1.1V	709
BV40	lpddr4_3_ch1_dq_b[2]	IO_L5N_N1P5_M3P11_709	1.1V	709
BU41	lpddr4_3_ch1_dq_b[5]	IO_L1N_N0P3_M3P3_709	1.1V	709
BU42	lpddr4_3_ch1_dq_b[7]	IO_L4P_N1P2_M3P8_709	1.1V	709
BV39	lpddr4_3_ch1_dq_b[0]	IO_L5P_N1P4_M3P10_709	1.1V	709
BH40	lpddr4_3_ch1_dqs_c_a[0]	IO_L12N_GC_XCC_N4P1_M3P25_709	1.1V	709
BV38	lpddr4_3_ch1_dqs_c_b[0]	IO_L3N_XCC_N1P1_M3P7_709	1.1V	709
BG39	lpddr4_3_ch1_dqs_t_a[0]	IO_L12P_GC_XCC_N4P0_M3P24_709	1.1V	709
BU38	lpddr4_3_ch1_dqs_t_b[0]	IO_L3P_XCC_N1P0_M3P6_709	1.1V	709
BM42	NC	IO_L24N_GC_XCC_N8P1_M3P49_709	1.1V	709
BL42	NC	IO_L24P_GC_XCC_N8P0_M3P48_709	1.1V	709
BM41	NC	IO_L25P_N8P2_M3P50_709	1.1V	709
BN39	NC	IO_L26N_N8P5_M3P53_709	1.1V	709
BP40	NC	IO_L7N_N2P3_M3P15_709	1.1V	709
BN40	NC	IO_L7P_N2P2_M3P14_709	1.1V	709
BM39	qsfp0_lpmode_1v1	IO_L26P_N8P4_M3P52_709	1.1V	709
BN41	qsfp0_reset_1v1_l	IO_L25N_N8P3_M3P51_709	1.1V	709
BM47	lpddr4_3_ch0_dmi_a[0]	IO_L6P_GC_XCC_N2P0_M3P66_710	1.1V	710

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BE46	lpddr4_3_ch0_dmi_b[0]	IO_L18P_XCC_N6P0_M3P90_710	1.1V	710
BV46	lpddr4_3_ch0_dq_a[0]	IO_L11N_N3P5_M3P77_710	1.1V	710
BR47	lpddr4_3_ch0_dq_a[7]	IO_L8N_N2P5_M3P71_710	1.1V	710
BU47	lpddr4_3_ch0_dq_a[6]	IO_L10N_N3P3_M3P75_710	1.1V	710
BV45	lpddr4_3_ch0_dq_a[3]	IO_L11P_N3P4_M3P76_710	1.1V	710
BN48	lpddr4_3_ch0_dq_a[4]	IO_L7P_N2P2_M3P68_710	1.1V	710
BP48	lpddr4_3_ch0_dq_a[5]	IO_L7N_N2P3_M3P69_710	1.1V	710
BP47	lpddr4_3_ch0_dq_a[2]	IO_L8P_N2P4_M3P70_710	1.1V	710
BU46	lpddr4_3_ch0_dq_a[1]	IO_L10P_N3P2_M3P74_710	1.1V	710
BJ48	lpddr4_3_ch0_dq_b[4]	IO_L22P_N7P2_M3P98_710	1.1V	710
BK47	lpddr4_3_ch0_dq_b[1]	IO_L23P_N7P4_M3P100_710	1.1V	710
BK48	lpddr4_3_ch0_dq_b[2]	IO_L22N_N7P3_M3P99_710	1.1V	710
BL47	lpddr4_3_ch0_dq_b[3]	IO_L23N_N7P5_M3P101_710	1.1V	710
BG47	lpddr4_3_ch0_dq_b[7]	IO_L20N_N6P5_M3P95_710	1.1V	710
BF48	lpddr4_3_ch0_dq_b[6]	IO_L19P_N6P2_M3P92_710	1.1V	710
BG48	lpddr4_3_ch0_dq_b[5]	IO_L19N_N6P3_M3P93_710	1.1V	710
BF46	lpddr4_3_ch0_dq_b[0]	IO_L20P_N6P4_M3P94_710	1.1V	710
BT47	lpddr4_3_ch0_dqs_c_a[0]	IO_L9N_GC_XCC_N3P1_M3P73_710	1.1V	710
BJ47	lpddr4_3_ch0_dqs_c_b[0]	IO_L21N_XCC_N7P1_M3P97_710	1.1V	710
BT46	lpddr4_3_ch0_dqs_t_a[0]	IO_L9P_GC_XCC_N3P0_M3P72_710	1.1V	710
BH47	lpddr4_3_ch0_dqs_t_b[0]	IO_L21P_XCC_N7P0_M3P96_710	1.1V	710
BT44	lpddr4_3_ch1_dmi_a[1]	IO_L3P_XCC_N1P0_M3P60_710	1.1V	710
BC45	lpddr4_3_ch1_dmi_b[1]	IO_L12P_GC_XCC_N4P0_M3P78_710	1.1V	710
BV43	lpddr4_3_ch1_dq_a[10]	IO_L5P_N1P4_M3P64_710	1.1V	710
BV44	lpddr4_3_ch1_dq_a[11]	IO_L5N_N1P5_M3P65_710	1.1V	710
BU43	lpddr4_3_ch1_dq_a[9]	IO_L4P_N1P2_M3P62_710	1.1V	710
BU44	lpddr4_3_ch1_dq_a[8]	IO_L4N_N1P3_M3P63_710	1.1V	710
BR45	lpddr4_3_ch1_dq_a[14]	IO_L2N_N0P5_M3P59_710	1.1V	710
BR44	lpddr4_3_ch1_dq_a[12]	IO_L2P_N0P4_M3P58_710	1.1V	710
BP45	lpddr4_3_ch1_dq_a[13]	IO_L1P_N0P2_M3P56_710	1.1V	710
BP46	lpddr4_3_ch1_dq_a[15]	IO_L1N_N0P3_M3P57_710	1.1V	710
BF45	lpddr4_3_ch1_dq_b[10]	IO_L14N_N4P5_M3P83_710	1.1V	710
BD44	lpddr4_3_ch1_dq_b[11]	IO_L13P_N4P2_M3P80_710	1.1V	710
BD45	lpddr4_3_ch1_dq_b[8]	IO_L13N_N4P3_M3P81_710	1.1V	710
BE44	lpddr4_3_ch1_dq_b[9]	IO_L14P_N4P4_M3P82_710	1.1V	710
BK44	lpddr4_3_ch1_dq_b[15]	IO_L17P_N5P4_M3P88_710	1.1V	710

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BK45	lpddr4_3_ch1_dq_b[14]	IO_L17N_N5P5_M3P89_710	1.1V	710
BJ46	lpddr4_3_ch1_dq_b[12]	IO_L16N_N5P3_M3P87_710	1.1V	710
BJ45	lpddr4_3_ch1_dq_b[13]	IO_L16P_N5P2_M3P86_710	1.1V	710
BN46	lpddr4_3_ch1_dqs_c_a[1]	IO_L0N_XCC_N0P1_M3P55_710	1.1V	710
BH46	lpddr4_3_ch1_dqs_c_b[1]	IO_L15N_XCC_N5P1_M3P85_710	1.1V	710
BN45	lpddr4_3_ch1_dqs_t_a[1]	IO_L0P_XCC_N0P0_M3P54_710	1.1V	710
BG45	lpddr4_3_ch1_dqs_t_b[1]	IO_L15P_XCC_N5P0_M3P84_710	1.1V	710
BC46	NC	IO_L12N_GC_XCC_N4P1_M3P79_710	1.1V	710
BE47	NC	IO_L18N_XCC_N6P1_M3P91_710	1.1V	710
BL45	NC	IO_L24N_GC_XCC_N8P1_M3P103_710	1.1V	710
BL44	NC	IO_L24P_GC_XCC_N8P0_M3P102_710	1.1V	710
BL46	NC	IO_L25P_N8P2_M3P104_710	1.1V	710
BN44	NC	IO_L26N_N8P5_M3P107_710	1.1V	710
BT45	NC	IO_L3N_XCC_N1P1_M3P61_710	1.1V	710
BM48	NC	IO_L6N_GC_XCC_N2P1_M3P67_710	1.1V	710
BM44	qsfp1_lpmode_1v1	IO_L26P_N8P4_M3P106_710	1.1V	710
BM46	qsfp1_reset_1v1_l	IO_L25N_N8P3_M3P105_710	1.1V	710
BU51	lpddr4_3_ch0_ca_a[0]	IO_L1N_N0P3_M3P111_711	1.1V	711
BT51	lpddr4_3_ch0_ca_a[1]	IO_L1P_N0P2_M3P110_711	1.1V	711
BR52	lpddr4_3_ch0_ca_a[2]	IO_L0P_XCC_N0P0_M3P108_711	1.1V	711
BU49	lpddr4_3_ch0_ca_a[3]	IO_L2N_N0P5_M3P113_711	1.1V	711
BU52	lpddr4_3_ch0_ca_a[4]	IO_L4P_N1P2_M3P116_711	1.1V	711
BV51	lpddr4_3_ch0_ca_a[5]	IO_L4N_N1P3_M3P117_711	1.1V	711
BM52	lpddr4_3_ch0_ca_b[0]	IO_L7P_N2P2_M3P122_711	1.1V	711
BR49	lpddr4_3_ch0_ca_b[1]	IO_L11N_N3P5_M3P131_711	1.1V	711
BP50	lpddr4_3_ch0_ca_b[2]	IO_L8N_N2P5_M3P125_711	1.1V	711
BN50	lpddr4_3_ch0_ca_b[3]	IO_L8P_N2P4_M3P124_711	1.1V	711
BT50	lpddr4_3_ch0_ca_b[4]	IO_L10N_N3P3_M3P129_711	1.1V	711
BR50	lpddr4_3_ch0_ca_b[5]	IO_L10P_N3P2_M3P128_711	1.1V	711
BV48	lpddr4_3_ch0_ck_c_a[0]	IO_L3N_XCC_N1P1_M3P115_711	1.1V	711
BP52	lpddr4_3_ch0_ck_c_b[0]	IO_L9N_GC_XCC_N3P1_M3P127_711	1.1V	711
BU48	lpddr4_3_ch0_ck_t_a[0]	IO_L3P_XCC_N1P0_M3P114_711	1.1V	711
BP51	lpddr4_3_ch0_ck_t_b[0]	IO_L9P_GC_XCC_N3P0_M3P126_711	1.1V	711
BV49	lpddr4_3_ch0_cke_a[0]	IO_L5P_N1P4_M3P118_711	1.1V	711
BV50	lpddr4_3_ch0_cke_a[1]	IO_L5N_N1P5_M3P119_711	1.1V	711
BR48	lpddr4_3_ch0_cke_b[0]	IO_L11P_N3P4_M3P130_711	1.1V	711

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BM53	lpddr4_3_ch0_cke_b[1]	IO_L7N_N2P3_M3P123_711	1.1V	711
BT49	lpddr4_3_ch0_cs_a[0]	IO_L2P_N0P4_M3P112_711	1.1V	711
BT52	lpddr4_3_ch0_cs_a[1]	IO_L0N_XCC_N0P1_M3P109_711	1.1V	711
BF50	lpddr4_3_ch0_cs_b[0]	IO_L21N_XCC_N7P1_M3P151_711	1.1V	711
BH53	lpddr4_3_ch0_cs_b[1]	IO_L12N_GC_XCC_N4P1_M3P133_711	1.1V	711
BG53	lpddr4_3_ch0_dmi_a[1]	IO_L12P_GC_XCC_N4P0_M3P132_711	1.1V	711
BF49	lpddr4_3_ch0_dmi_b[1]	IO_L21P_XCC_N7P0_M3P150_711	1.1V	711
BH51	lpddr4_3_ch0_dq_a[13]	IO_L13N_N4P3_M3P135_711	1.1V	711
BH50	lpddr4_3_ch0_dq_a[12]	IO_L13P_N4P2_M3P134_711	1.1V	711
BJ50	lpddr4_3_ch0_dq_a[9]	IO_L14P_N4P4_M3P136_711	1.1V	711
BJ51	lpddr4_3_ch0_dq_a[14]	IO_L14N_N4P5_M3P137_711	1.1V	711
BK49	lpddr4_3_ch0_dq_a[8]	IO_L17P_N5P4_M3P142_711	1.1V	711
BK50	lpddr4_3_ch0_dq_a[15]	IO_L17N_N5P5_M3P143_711	1.1V	711
BK53	lpddr4_3_ch0_dq_a[11]	IO_L16N_N5P3_M3P141_711	1.1V	711
BK52	lpddr4_3_ch0_dq_a[10]	IO_L16P_N5P2_M3P140_711	1.1V	711
BG51	lpddr4_3_ch0_dq_b[14]	IO_L23P_N7P4_M3P154_711	1.1V	711
BG49	lpddr4_3_ch0_dq_b[8]	IO_L22P_N7P2_M3P152_711	1.1V	711
BF52	lpddr4_3_ch0_dq_b[11]	IO_L20N_N6P5_M3P149_711	1.1V	711
BE53	lpddr4_3_ch0_dq_b[9]	IO_L19N_N6P3_M3P147_711	1.1V	711
BF51	lpddr4_3_ch0_dq_b[10]	IO_L20P_N6P4_M3P148_711	1.1V	711
BE52	lpddr4_3_ch0_dq_b[13]	IO_L19P_N6P2_M3P146_711	1.1V	711
BH49	lpddr4_3_ch0_dq_b[15]	IO_L22N_N7P3_M3P153_711	1.1V	711
BG52	lpddr4_3_ch0_dq_b[12]	IO_L23N_N7P5_M3P155_711	1.1V	711
BJ53	lpddr4_3_ch0_dqs_c_a[1]	IO_L15N_XCC_N5P1_M3P139_711	1.1V	711
BE50	lpddr4_3_ch0_dqs_c_b[1]	IO_L18N_XCC_N6P1_M3P145_711	1.1V	711
BJ52	lpddr4_3_ch0_dqs_t_a[1]	IO_L15P_XCC_N5P0_M3P138_711	1.1V	711
BE49	lpddr4_3_ch0_dqs_t_b[1]	IO_L18P_XCC_N6P0_M3P144_711	1.1V	711
BL51	lpddr4_3_ch0_reset_n[0]	IO_L25P_N8P2_M3P158_711	1.1V	711
BL52	lpddr4_3_ch1_reset_n[0]	IO_L25N_N8P3_M3P159_711	1.1V	711
BL50	mem_clk_3_n	IO_L24N_GC_XCC_N8P1_M3P157_711	1.1V	711
BL49	mem_clk_3_p	IO_L24P_GC_XCC_N8P0_M3P156_711	1.1V	711
BG58	10mhz_n	IO_L12N_GC_XCC_N4P1_712	1.5V	712
BG57	10mhz_p	IO_L12P_GC_XCC_N4P0_712	1.5V	712
BL56	1pps_fpga	IO_L25P_N8P2_712	1.5V	712
BL54	485_0_data_fpga	IO_L26P_N8P4_712	1.5V	712
BN53	485_0_de/re_l_fpga	IO_L10P_N3P2_712	1.5V	712

Table 12 : Complete Pinout Table (continued on next page)

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BL55	485_1_data_fpga	IO_L26N_N8P5_712	1.5V	712
BP55	485_1_de/re_l_fpga	IO_L11P_N3P4_712	1.5V	712
BP57	avr_b2u_1v5	IO_L0P_XCC_N0P0_712	1.5V	712
BR55	avr_mon_clk_1v5	IO_L1P_N0P2_712	1.5V	712
BR57	avr_u2b_1v5	IO_L0N_XCC_N0P1_712	1.5V	712
BN55	fabric_clk_1v5	IO_L9P_GC_XCC_N3P0_712	1.5V	712
BP58	perst_pl_l	IO_L8N_N2P5_712	1.5V	712
BE54	pmod_io1_1v5	IO_L20P_N6P4_712	1.5V	712
BE55	pmod_io2_1v5	IO_L20N_N6P5_712	1.5V	712
BF54	pmod_io3_1v5	IO_L21P_XCC_N7P0_712	1.5V	712
BF55	pmod_io4_1v5	IO_L21N_XCC_N7P1_712	1.5V	712
BF56	pmod_io5_1v5	IO_L22P_N7P2_712	1.5V	712
BG56	pmod_io6_1v5	IO_L22N_N7P3_712	1.5V	712
BG54	pmod_io7_1v5	IO_L23P_N7P4_712	1.5V	712
BH54	pmod_io8_1v5	IO_L23N_N7P5_712	1.5V	712
BH56	qsfp0_scl_1v5	IO_L14N_N4P5_712	1.5V	712
BH55	qsfp0_sda_1v5	IO_L14P_N4P4_712	1.5V	712
BJ55	qsfp1_scl_1v5	IO_L15P_XCC_N5P0_712	1.5V	712
BJ56	qsfp1_sda_1v5	IO_L15N_XCC_N5P1_712	1.5V	712
BJ57	qsfp2_scl_1v5	IO_L16P_N5P2_712	1.5V	712
BK57	qsfp2_sda_1v5	IO_L16N_N5P3_712	1.5V	712
BJ58	si5344_in0_n	IO_L13N_N4P3_712	1.5V	712
BH58	si5344_in0_p	IO_L13P_N4P2_712	1.5V	712
BD58	si5344_intr_1v5_n	IO_L18P_XCC_N6P0_712	1.5V	712
BE57	si5344_lol_1v5_n	IO_L19P_N6P2_712	1.5V	712
BF57	si5344_lol_xaxb_1v5_n	IO_L19N_N6P3_712	1.5V	712
BE58	si5344_rst_1v5_n	IO_L18N_XCC_N6P1_712	1.5V	712
BK55	si5344_scl_1v5	IO_L17N_N5P5_712	1.5V	712
BK54	si5344_sda_1v5	IO_L17P_N5P4_712	1.5V	712
BN58	si5402_1v5_scl	IO_L8P_N2P4_712	1.5V	712
BM58	si5402_1v5_sda	IO_L7N_N2P3_712	1.5V	712
BV53	si5402_gpio0_1v5	IO_L5P_N1P4_712	1.5V	712
BV54	si5402_gpio1_1v5	IO_L5N_N1P5_712	1.5V	712
BM57	si5402_gpio2_1v5	IO_L7P_N2P2_712	1.5V	712
BU54	si5402_in0_n	IO_L4N_N1P3_712	1.5V	712
BU53	si5402_in0_p	IO_L4P_N1P2_712	1.5V	712

Table 12 : Complete Pinout Table **(continued on next page)**

Pin Number	Signal Name	Pin Name	IO Voltage	Bank
BT55	si5402_in1_n	IO_L3N_XCC_N1P1_712	1.5V	712
BT54	si5402_in1_p	IO_L3P_XCC_N1P0_712	1.5V	712
BR54	si5402_in2_n	IO_L2N_N0P5_712	1.5V	712
BR53	si5402_in2_p	IO_L2P_N0P4_712	1.5V	712
BN54	si5402_out5_n	IO_L6N_GC_XCC_N2P1_712	1.5V	712
BM54	si5402_out5_p	IO_L6P_GC_XCC_N2P0_712	1.5V	712
BT56	si5402_rst_1v5_n	IO_L1N_N0P3_712	1.5V	712
BN56	srvc_md_l_1v5	IO_L9N_GC_XCC_N3P1_712	1.5V	712
BP53	trig_in_fpga	IO_L10N_N3P3_712	1.5V	712
BP56	trig_out_en_fpga	IO_L11N_N3P5_712	1.5V	712
BM56	trig_out_fpga	IO_L25N_N8P3_712	1.5V	712
BL57	trig_te_en_fpga	IO_L24N_GC_XCC_N8P1_712	1.5V	712
BK58	usr_sw_0	IO_L24P_GC_XCC_N8P0_712	1.5V	712

Table 12 : Complete Pinout Table

Revision History

Date	Revision	Changed By	Nature of Change
15 Aug 2025	1.0	J. Wood	First release

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